Product Description

Do-Networks's OSFP 8x100Gbps transceiver module can be used for 800 Gigabit Ethernet connections over 2km of single-mode fiber. The module includes eight parallel channels with a central wavelength of 1310nm, and the operating rate of each channel is 106.25Gbps. These 8-channel PAM4 parallel optical signals can be converted into 8-channel PAM4 electrical output signals; and there are 8 independent electrical input/output channels, which can convert PAM4 electrical input data into 8-channel PAM4 parallel optical signal. The transmitter of the module includes a bi-directional PAM4 re-timer ASIC with an 8-channel modulator driver and 8 EML Lasers. The receiver uses 8 photodiodes and integrated TIA, as well as the PAM4 re-timer. The electrical interface of the module is compliant with the 800GAUI-8 interface as defined by IEEE 802.3ck, and compliant with OSFP MSA.

Features

- Supports 850Gbps
- Single 3.3V Power Supply
- Up to 2km over SMF with KP4 FEC supported at the Host side
- Dual MPO-12 connector
- 8x106.25Gbps (PAM4) electrical interface
- Driver and TIA integrated in the DSP at transmitter and receiver side
- Power dissipation < 14.5W
- Case temperature range: 0°C to 70°C (commercial)
- Safety Certification: TUV/UL/FDA*1
- RoHS Compliant

Applications*1

- 8x100G Ethernet
- 2x400G Ethernet
- 1x800G Ethernet

Ordering Information

Part No.	Data Rate	Fiber	Distance*2	Interface	Temp.	DDMI	CMIS
800G-OSFP112-2xDR4+	850Gbps	SMF	2km	Dual MPO-12	0~70°C	Yes	CMIS5.0*3

*1: For more details, please contact with Do-Networks.
*2: Over G.652 SMF.
*3: CMIS5.0 or later version.

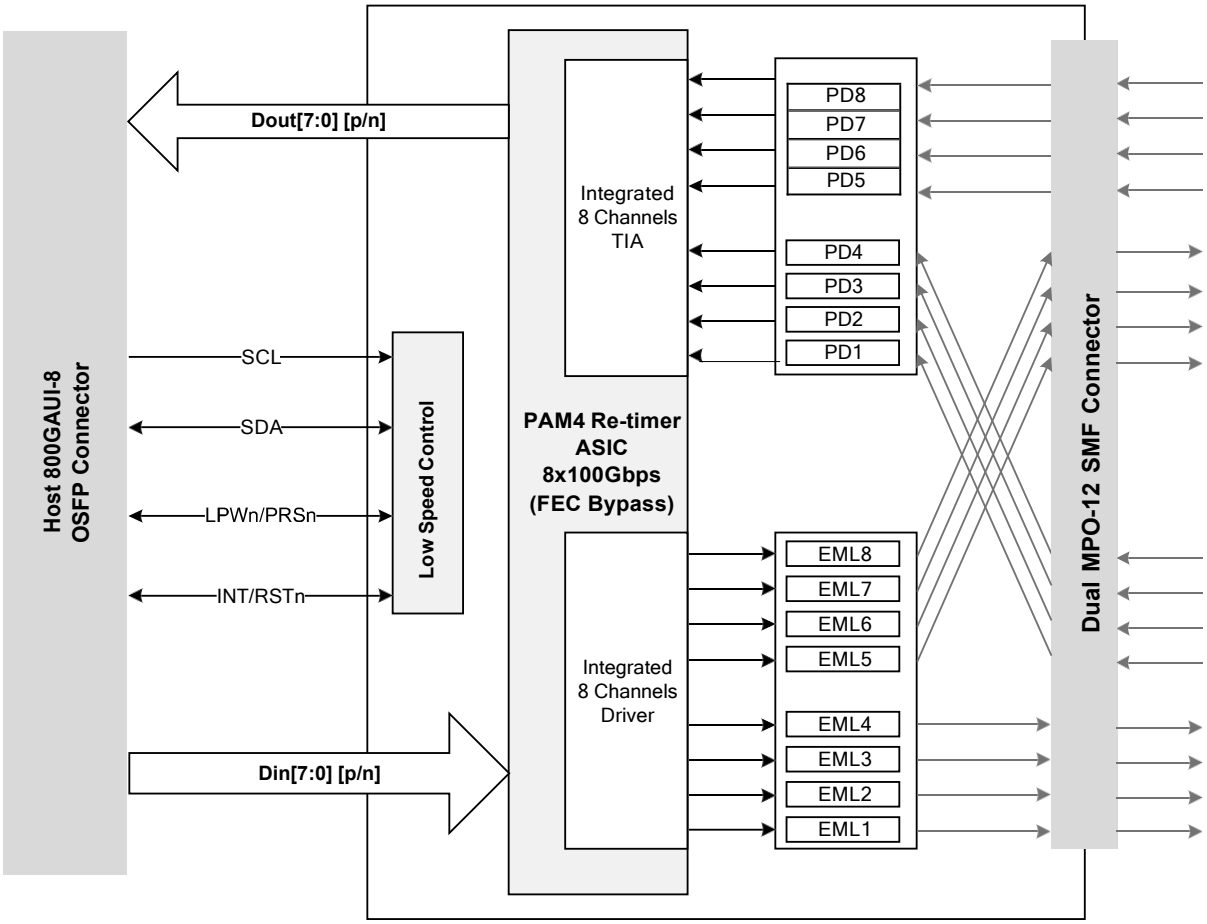

Figure 1: Transceiver Block Diagram

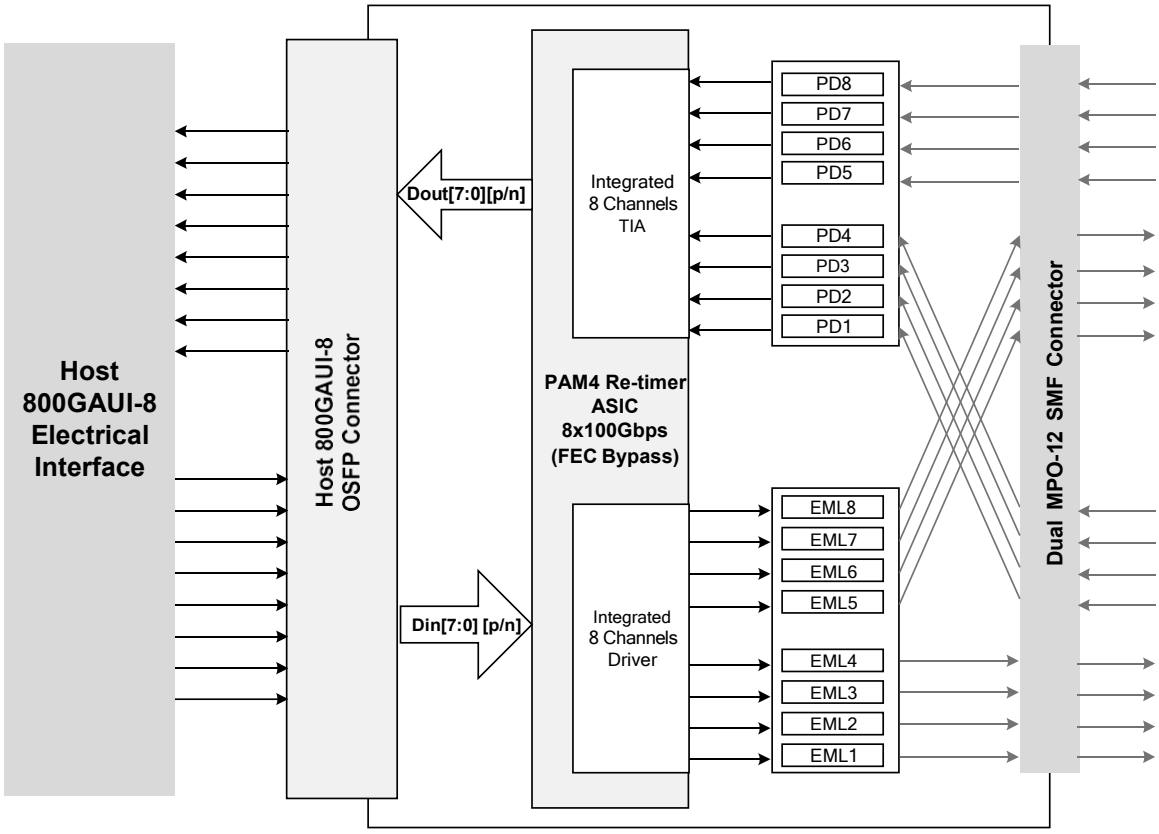

Figure 2: Application Reference Diagram

Transmitter

As shown in Figure 1, the transmitter path of the transceiver contains an 8x100Gbps 800GAUI-8 electrical input with Equalization (EQ) block, integrated electrical multiplexer, integrated EML driver, diagnostic monitors and 8 single mode EML lasers. The integrated electrical multiplexer and integrated EML driver converts 8 channels of 100 Gbps (PAM4) electrical input data to 8 channels of 100Gbps (PAM4) parallel optical signals. The transmitter complies with EN 60825 and CDRH Class 1 human eye safety compliance.

Receiver

As shown in Figure 1, the receiver path of the transceiver contains eight PIN photodiodes, integrated trans-impedance amplifiers (TIA), integrated de-multiplexer and 8x100G 800GAUI-8 compliant electrical output blocks. The PIN, integrated TIA and de-multiplexer converts 8 channels of 100Gbps (PAM4) parallel optical signals to 8 channels of 100Gbps (PAM4) electrical output data.

High Speed Electrical Signal Interface

The Application Reference Diagram shown in Figure2 illustrated the interface between the OSFP module and Host 800GAUI-8. The high speed signal lines are internally AC-coupled and the electrical inputs are internally terminated to 100 Ohms differential. All transmitter and receiver electrical channels are compliant to module 800GAUI-8 specifications per IEEE 802.3ck.

Control Signal Interface

The ModPrsL, IntL/RxLOS, ResetL, LPMode/TxDis are the low speed signals for control and status. In addition, there is an industry standard two wire serial interface scaled for 3.3V LVTTL. It is implemented as a slave device. Signal and timing characteristics are further defined in the Control Interface& Memory map sections.
The registers of the serial interface memory are defined in the Control Interface & Memory map section.

Handling and Cleaning

The transceiver module may be damaged immediately due to current surge and overvoltage; Observe the precautions for normal operation of electrostatic discharge sensitive equipment; Attention shall also be paid to limiting transceiver module exposure to conditions beyond those specified in the absolute maximum ratings.
Optical connectors include female connectors. These elements will be exposed as long as the cable or port plug is not inserted. At this time, always pay attention to protection.
Each module is equipped with a port guard plug to protect the optical port. The protective plug shall always be in place whenever the optical fiber is not inserted. Before inserting the optical fiber, it is recommended to clean the end of the optical fiber connector to avoid contamination of the module optical port due to dirty connector. If contamination occurs, use standard MPO port cleaning methods.

Absolute Maximum Ratings

Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operating Conditions. It should not be assumed that limiting values of more than one parameter can be applied to the module concurrently. Exposure to any of the Absolute Maximum Ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage Temperature	Ts	-40		85	°C
3.3 V Power Supply Voltage	Vcc	-0.5	3.3	3.6	V
Data Input Voltage – Single Ended		-0.5		Vcc+0.5	V
Data Input Voltage – Differential*4				0.8	V
Relative Humidity	RH	5		85	%

*4: This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry. The damage threshold of the module input shall be at least 1600 mV peak to peak differential.

Recommended Operating Conditions*5

Recommended Operating Conditions specify parameters for which the optical and electrical characteristics hold unless otherwise noted. Optical and electrical characteristics are not defined for operation outside the Recommended Operating Conditions, reliability is not implied and damage to the module may occur for such operation over an extended period of time.

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating case temperature*6	Tc	0		70	°C
Power supply voltage	Vcc	3.135	3.3	3.465	V
Power dissipation	P_D			14.5	W
Electrical Signal Rate per Channel (PAM encoded)*7			53.125		GBd
Optical Signal Rate per Channel (PAM encoded)*8			53.125		GBd
Power Supply Noise*9				66	mVpp
Receiver Differential Data Output Load		100			Ohm
Fiber Length (9μm SMF)*10				2000	m

*5: Power Supply specifications, Instantaneous, sustained and steady state current compliant with OSFP MSA Power Classification.

*6: The position of case temperature measurement is shown in Figure 9.

*7: 800GAUI-8 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.

*8: 8×100G-FR operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.

*9: Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 7 for recommended power supply filter.

*10: 9μm SMF. The maximum link distance is based on an allocation of 1dB of attenuation and 3dB total connection and splice loss. The loss of a single connection shall not exceed 0.5dB.

General Electrical Characteristics*11

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Symbol	Min.	Typical	Max.	Unit
Transceiver Power Consumption			13.5	14.5	W
Transceiver Power Supply Current, Total			4310	4630	mA
AC coupling capacitors (Internal)			0.1		µF

*11: For control signal timing including ModSelL, ResetL, LPMode/TxDisable, ModePrsL, IntL/RxLOSL, SCL and SDA see Control Interface Section.

Reference Points

Test Point	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are made between TP1 and TP4 as illustrated in Figure 3.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 802.3ck 162.9.3 and 162.9.4. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided in 802.3ck 162.9.3.2
TP2	Unless specified otherwise, all transmitter measurements defined in 802.3ck 162.9.3 are made at TP2 utilizing the test fixture specified in Annex 162B.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 802.3ck 162.9.4 are made at TP3 utilizing the test fixture specified in Annex 162B.

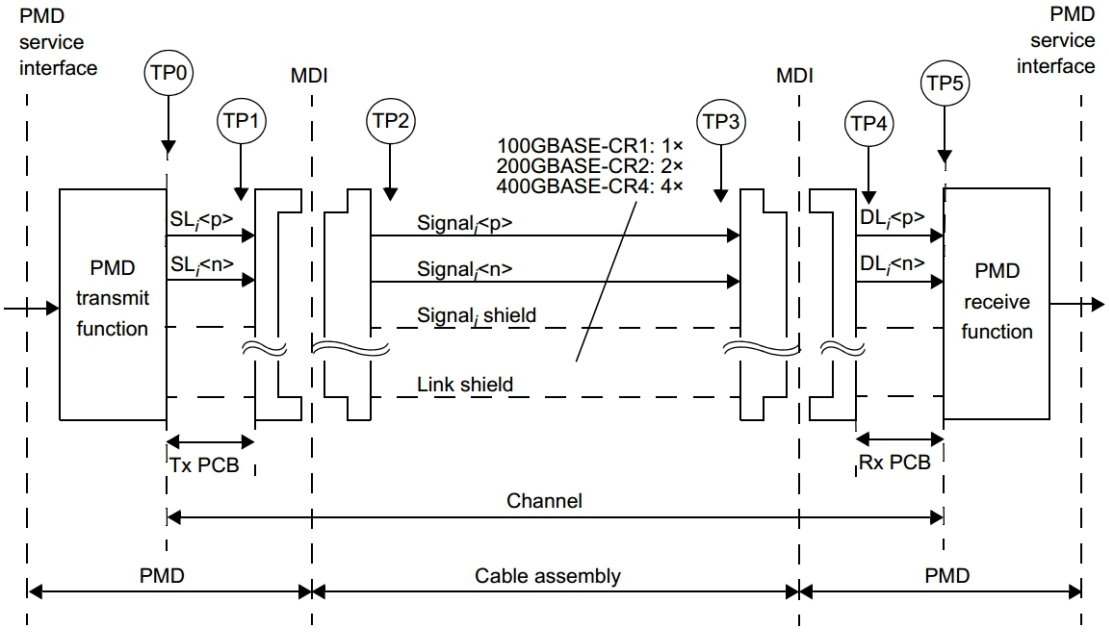

Figure 3: IEEE 802.3ck 100GBASE-CR1, 200GBASE-CR2 or 400GBASE-CR4 link

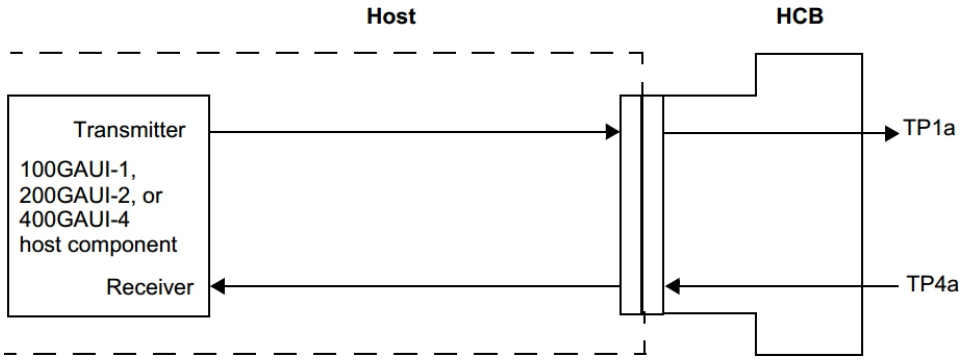

Figure 4: IEEE 802.3ck host compliance points TP1a, TP4a

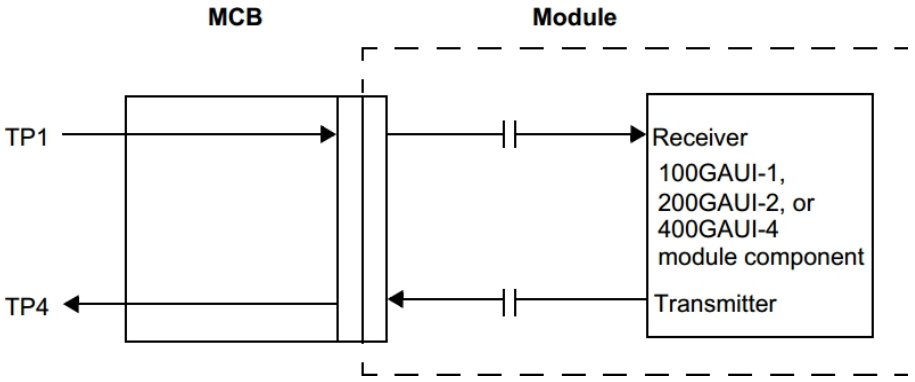

Figure 5: IEEE 802.3ck module compliance points TP1, TP4

High Speed Electrical Input Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point	Min.	Typical	Max.	Unit	Conditions
Signaling Rate, Per Lane (PAM4 encoded)	TP1		53.125		GBd	+/- 100 ppm
Differential peak-peak Input Voltage Tolerance	TP1a	750			mV	
AC common-mode RMS voltage tolerance	TP1a	25			mV	
Differential-mode to common-mode return loss	TP1	Equation (120G-2)			dB	802.3ck
Effective return loss, ERL	TP1	8.5			dB	
Differential termination mismatch	TP1			10	%	
Module stressed input tolerance	TP1a		See 120G.3.4.3			802.3ck
Single-ended voltage tolerance range	TP1a	-0.4		3.3	V	
DC common-mode voltage tolerance range	TP1	-350		2850	mV	
Module stressed input tolerance test :						

Pattern generator transition time		9		ps
Applied peak-peak sinusoidal jitter		Table 162-16		802.3ck
Eye height		10		mV
Vertical eye closure, VEC	12		12.5	dB
Crosstalk differential peak-to-peak voltage		845		mV
Crosstalk transition time		8.5		ps

High Speed Electrical Output Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point	Min.	Typical	Max.	Unit
Signaling Rate, Per Lane (range)	TP4		53.125*12 ± 100 ppm		GBd
AC common-mode output voltage	TP4			25	mV
Differential peak-to-peak input voltageShort mode Long mode	TP4			600 845	mV
Eye height	TP4	15			mV
Vertical eye closure	TP4			12	dB
Effective return loss	TP4	8.5			dB
Common-mode to differential-mode return loss	TP4	Equation (120G-1)			dB
Differential termination mismatch	TP4			10	%
Transition time	TP4	8.5			ps
DC common-mode voltage tolerance	TP4	-0.35		2.85	V

*12: The signaling rate range is derived from the PMD receiver input.

High Speed Optical Transmitter Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Optical Characteristics @TP2 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling speed per lane			106.25		Gbps
Modulation format			PAM4		
Center wavelength	λ	1304.5	1311	1317.5	nm

Side-mode Suppression Ratio	SMSR	30		dB
Extinction ratio	ER	3.5		dB
Average launch power*13		-2.4	4	dBm
OMA_{outer} per lane		-0.2	4.2	dBm
Launch Power in OMA-TDECQ For Extinction Ratio ≥ 4.5 dB For Extinction Ratio < 4.5 dB		 -1.6 -1.5		dBm
TDECQ (PAM4)			3.4	dB
TECQ			3.4	dB
$RIN_{17.1}$ OMA			-136	dB/Hz
Average launch power of OFF transmitter			-15	dBm
Optical return loss tolerance			17.1	dB
Transmitter Reflectance			-26	dB

*13: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

High Speed Optical Receiver Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Optical Characteristics @TP3 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling speed per lane			106.25		Gbps
Center wavelength	λ	1305.5	1311	1317.5	nm
Damage threshold		5.5			dBm
Average receiver power per lane		-6.4		4.5	dBm
Saturation receive power (OMA_{outer}) per Lane				4.7	dBm
Unstressed Receiver Sensitivity (OMA) Per Lane For TECQ < 1.4 dB For 1.4 dB≤ TECQ ≤ 3.4 dB	Sen*14			 -4.5 TECQ-5.9	dBm
LOS Assert (Avg.)	LOSA	-15			dBm
LOS De-Assert (Avg.)	LOSD			-10	dBm
RSSI accuracy		-2		+2	dB
Receiver reflectance				-26	dB

*14: Measured with conformance test signal at TP3 for the BER specified in IEEE Std 802.3cd clause 140.1.1.

Regulatory & Compliance Issues

Various standard and regulations apply to the 800G-OSFP112-2xDR4+ modules. These include eye-safety, Component Recognition, RoHS, ESD, EMC and Immunity. Please note the transmitter module is a Class 1 laser product. See Regulatory Compliance Table for details.

Regulatory Compliance Table

Feature	Test Method	Performance
Laser Eye Safety and Equipment Type Testing 	(IEC) EN 62368-1:2014+A11 (IEC) EN 60825-1:2014 (IEC) EN 60825-2:2004+A1+A2	CDRH Accession Number:2132182-000TUV File: R 50457725 0001 CB File: JPTUV-100513
Component Recognition	Underwriters Laboratories (UL) and Canadian Standards Association (CSA) Joint Component Recognition for InformationTechnology Equipment including Electrical Business Equipment	UL File: E317337
RoHS Compliance	RoHS Directive 2011/65/EU&(EU)2015/863	Less than 100 ppm of cadmium. Less than 1000 ppm lead, mercury, hexavalent chromium, poly brominated biphenyls (PPB) , poly brominated biphenyl ethers (PBDE), dibutyl phthalate, butyl benzyl phthalate, bis (2-ethylhexyl) phthalate and diisobutyl phthalates.
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM)	High speed contacts shall withstand 1000V. All other contacts shall withstand 2000 V.
Electrostatic Discharge (ESD) to the Optical Connector Receptacle	IEC 61000-4-2:2008	When installed in a properly grounded housing and chassis the units are subjected to 15kV air discharges during operation and 8kV direct discharges to the case.
Electromagnetic Interference (EMI)	FCC Part 15 Class B; CISPR 32 (EN55032) 2015;	System margins are dependent on customer board and chassis design.
Immunity	IEC 61000-4-3:2010; EN55035:2017	Typically shows no measurable effect from a 10V/m field swept from 80 MHz to 6 GHz applied to the module without a chassis enclosure.

Electrostatic Discharge (ESD)

800G-OSFP112-2xDR4+ complies with the ESD requirements described in the Regulatory Compliance Table. However, in the normal processing and operation of optical transceiver, the following two types of situations need special attention.

Case I: Before inserting the transceiver into the rack meeting the requirements of OSFP MSA, ESD preventive measures must be taken to protect the equipment. For example, the grounding wrist strap, workbench and floor should be used wherever the transceiver is handled.

Case II: After the transceiver is installed, the electrostatic discharge outside the chassis of the host equipment shall be within the scope of system level ESD requirements. If the optical interface of the transceiver is exposed outside the host equipment cabinet, the transceiver may be subject to equipment system level ESD requirements.

Electromagnetic Interference (EMI)

Communication equipment with optical transceivers is usually regulated by FCC in the United States and CENELEC EN55032 (CISPR 32) in Europe. The compliance of 800G-OSFP112-2xDR4+ with these standards is detailed in the regulatory compliance table. The metal shell and shielding design of EOLO-138HG-02- D2 will help equipment designers minimize the equipment level EMI challenges they face.

Flammability

800G-OSFP112-2xDR4+ optical transceiver meets UL certification requirements, its constituent materials have heat and corrosion resistance, and the plastic parts meet UL94V-0 requirements.

OSFP Transceiver Electrical Pad Layout

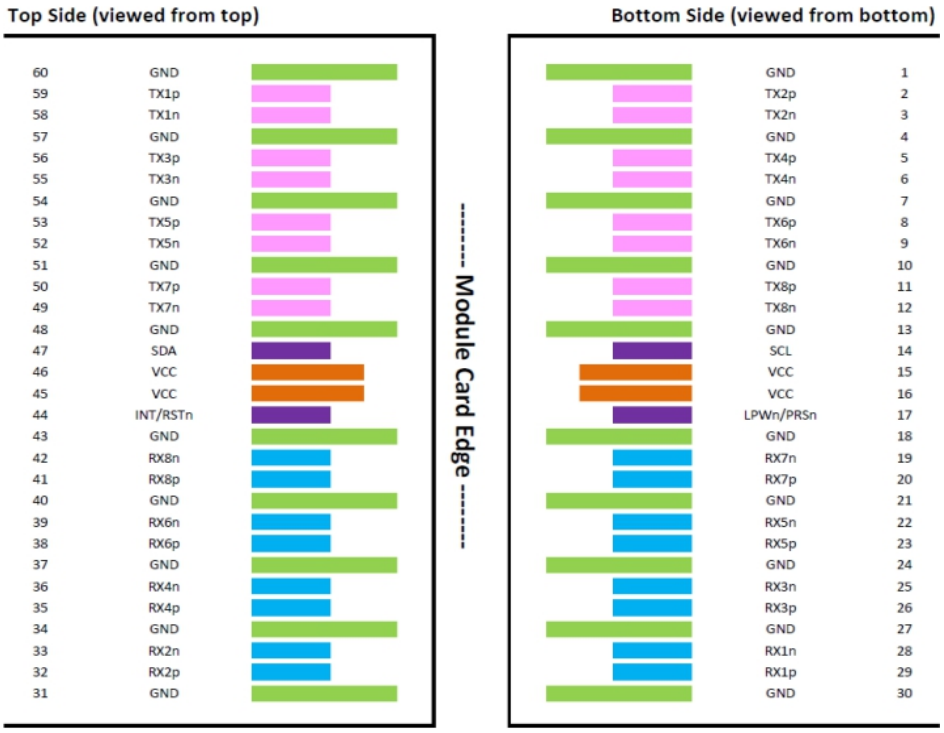

Figure 6: OSFP Module Pinout

Pin Arrangement and Definition

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2p	Transmitter Data Non-Inverted	3	
3	CML-I	Tx2n	Transmitter Data Inverted	3	
4		GND	Ground	1	1
5	CML-I	Tx4p	Transmitter Data Non-Inverted	3	
6	CML-I	Tx4n	Transmitter Data Inverted	3	
7		GND	Ground	1	1
8	CML-I	Tx6p	Transmitter Data Non-Inverted	3	
9	CML-I	Tx6n	Transmitter Data Inverted	3	
10		GND	Ground	1	1
11	CML-I	Tx8p	Transmitter Data Non-Inverted	3	
12	CML-I	Tx8n	Transmitter Data Inverted	3	
13		GND	Ground	1	1
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	3	2
15		VCC	+3.3V Power	2	
16		VCC	+3.3V Power	2	

17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present	3	
18		GND	Ground	1	1
19	CML-O	Rx7n	Receiver Data Inverted	3	
20	CML-O	Rx7p	Receiver Data Non-Inverted	3	
21		GND	Ground	1	1
22	CML-O	Rx5n	Receiver Data Inverted	3	
23	CML-O	Rx5p	Receiver Data Non-Inverted	3	
24		GND	Ground	1	1
25	CML-O	Rx3n	Receiver Data Inverted	3	
26	CML-O	Rx3p	Receiver Data Non-Inverted	3	
27		GND	Ground	1	1
28	CML-O	Rx1n	Receiver Data Inverted	3	
29	CML-O	Rx1p	Receiver Data Non-Inverted	3	
30		GND	Ground	1	1
31		GND	Ground	1	1
32	CML-O	Rx2p	Receiver Data Non-Inverted	3	
33	CML-O	Rx2n	Receiver Data Inverted	3	
34		GND	Ground	1	1
35	CML-O	Rx4p	Receiver Data Non-Inverted	3	
36	CML-O	Rx4n	Receiver Data Inverted	3	
37		GND	Ground	1	1
38	CML-O	Rx6p	Receiver Data Non-Inverted	3	
39	CML-O	Rx6n	Receiver Data Inverted	3	
40		GND	Ground	1	1
41	CML-O	Rx8p	Receiver Data Non-Inverted	3	
42	CML-O	Rx8n	Receiver Data Inverted	3	
43		GND	Ground	1	1
44	Multi-Level	INT/RSTn	Module input/Module Reset	3	
45		VCC	+3.3V Power	2	
46		VCC	+3.3V Power	2	
47	LVCMOS-I/O	SCL	2-wire Serial interface Data	3	2
48		GND	Ground	1	1
49	CML-I	Tx7n	Transmitter Data Inverted	3	
50	CML-I	Tx7p	Transmitter Data Non-Inverted	3	
51		GND	Ground	1	1
52	CML-I	Tx5n	Transmitter Data Inverted	3	
53	CML-I	Tx5p	Transmitter Data Non-Inverted	3	
54		GND	Ground	1	1
55	CML-I	Tx3n	Transmitter Data Inverted	3	
56	CML-I	Tx3p	Transmitter Data Non-Inverted	3	

57		GND	Ground	1	1
58	CML-I	Tx1n	Transmitter Data Inverted	3	
59	CML-I	Tx1p	Transmitter Data Non-Inverted	3	
60		GND	Ground	1	1
1: OSFP uses common ground (GND) for all signals and supply (power). All are common within the OSFP module and all module voltages are referenced to this potential unless otherwise noted.					
2: Open-Drain with pull up resistor on Host.					

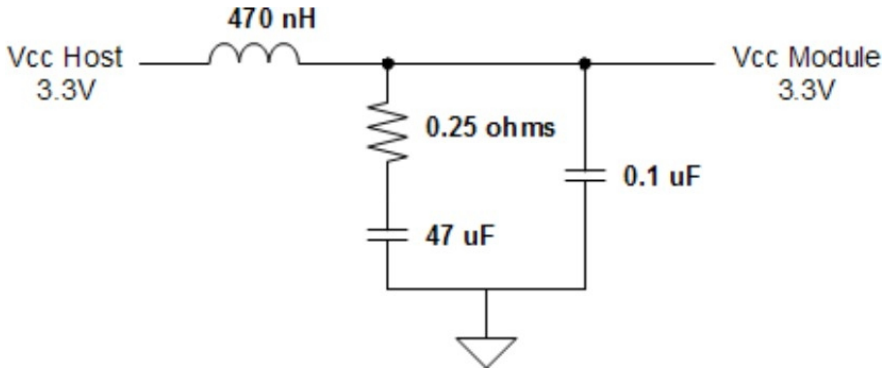

Figure 7: Recommended Host Board Power Supply Filter

For safety and protection of the host system, the power to each OSFP module may be protected by an electronic circuit breaker on the host board which is enabled with the H_PRSn signal such that power is only enabled when the module is fully engaged into the OSFP connector.

Package Outline

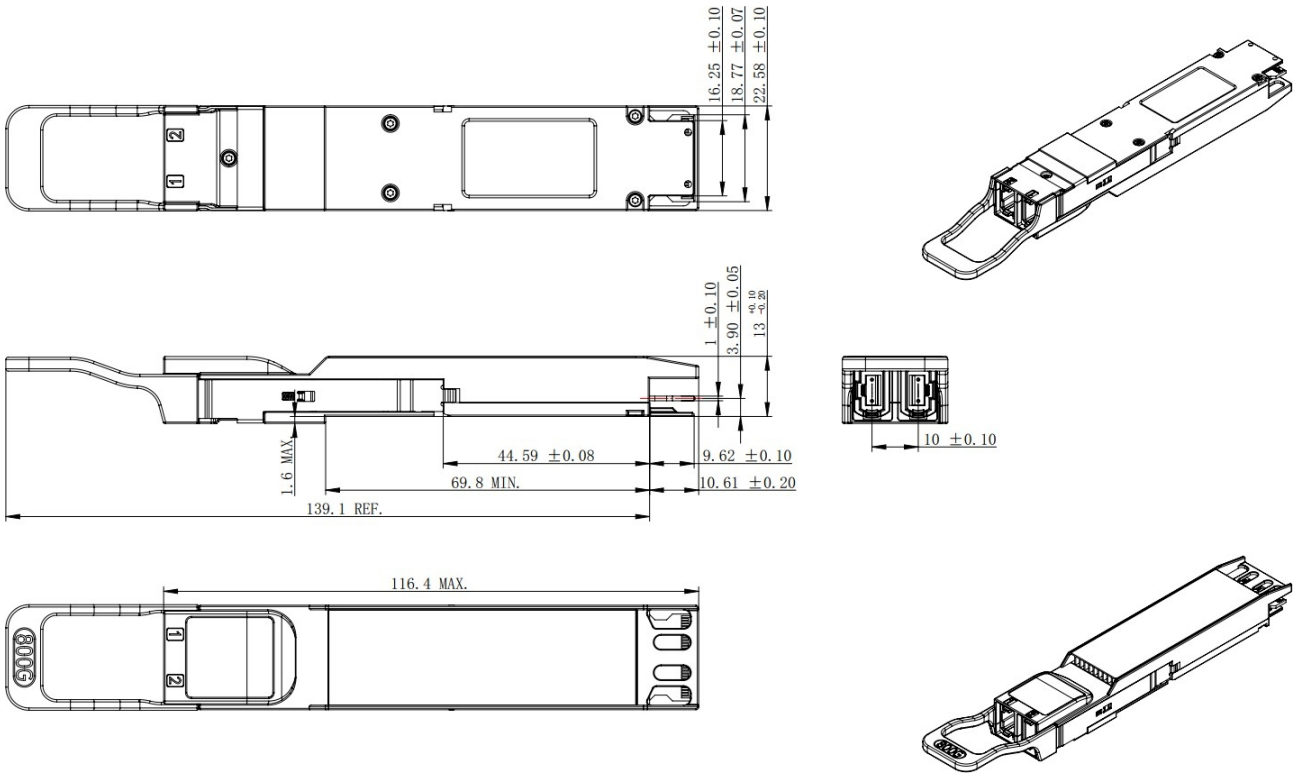

Figure 8: Mechanical Package Outline (All dimensions in mm)

*This 2D drawing is only for reference, please check with Do-Networks before ordering.

The bellow picture shows the location of the hottest spot for measuring module case temperature. In addition, the digital diagnostic monitors (DDM) temperature is also calibrated to this spot.

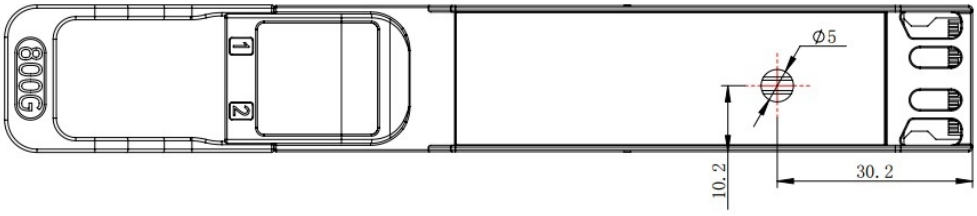

Figure 9: Case Temperature Measurement Point (All dimensions in mm)

The optical interface port is a male Dual MPO-12 connector. Mates with two standard type MPO-12 female plug connectors with down-angled interface.

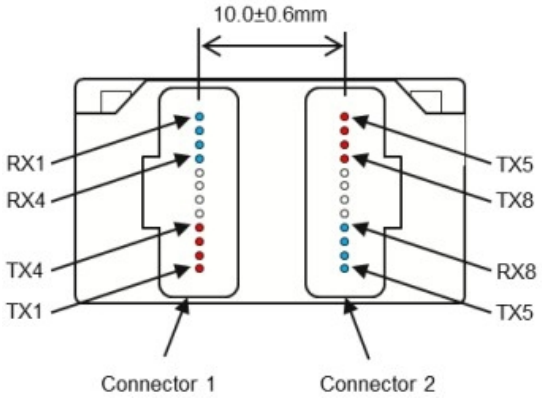

Figure 10: Module Optical Interface (looking into the optical port)

Control Interface & Memory Map

The control interface combines dedicated signal lines for LPWn/PRSn, INT/RSTn with two-wire serial (TWS), interface clock (SCL) and data (SDA), signals to provide users rich functionality over an efficient and easily used interface.

SCL and SDA

SCL and SDA are a 2-wire serial interface between the host and module using the I2C or I3C protocols. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3Von the host. The pull-up resistor value shall be 1k ohms to 4.7k ohms depending on capacitive load.

This 2-wire interface supports bus speeds:

- Required - I2C Fast-mode (Fm) ≤ 400 kbit/s
- Optional - I2C Fast-mode Plus (Fm+) ≤ 1 Mbit/s
- Optional - I3C Single Data Rate (SDR) ≤ 12.5 Mbit/s

The host shall default to using 100 kbit/s standard-mode I2C when first accessing an unidentified module for backward compatibility. Once the module has been brought out of reset, the host can read the module's 2-wire interface speed register to determine the maximum supported speed the module allows. For an OSFP, the host may then use I2C Fast-mode, I2C Fast-mode Plus or I3C Single Data Rate, as indicated by the module. It is optional for the host to change the speed of the 2-wire interface but remaining at a low speed could lead to slow management transactions for modules that require frequent accesses.

SCL and SDA signals follow the electrical specifications of Fast-mode, and Fast-mode Plus as defined in the I2C -bus specification or Single Data Rate mode as defined in the Specification for I3C.

SCL and SDA Pin Electrical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit
SCL and SDA	VOL	0		0.4	V
	VOH	VCC-0.5		VCC+0.3	V
SCL and SDA	VIL	-0.3		VCC*0.3	V
	VIH	VCC*0.7		VCC+0.5	V

INT/RSTn

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. The circuit shown in OSFP MSA Figure11-3 enables multi-level signaling to provide direct signal control in both directions. Reset is an active low signal on the host which is translated to an active-low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active-low signal on the host.

The INT/RSTn signal operates in 3 voltage zones to indicate the state of Reset for the module and Interrupt for the host. Figure 11 shows these 3 zone

s. The host uses a voltage reference at 2.5 volts to determine the state of the H_INTn signal and the module uses a voltage reference at 1.25V to determine the state of the M_RSTn signal.

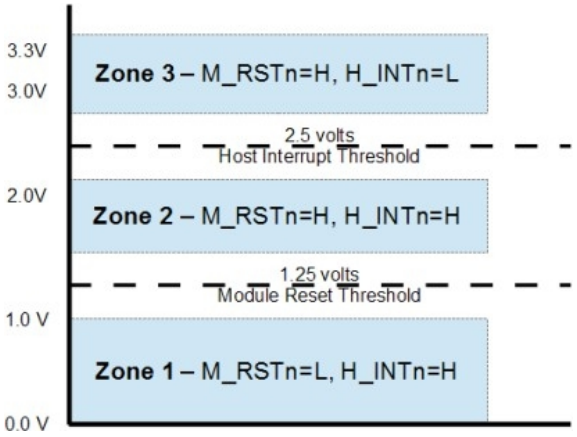

Figure 11: INT/RSTn Voltage Zones

LPWn/PRSn

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. The circuit shown in OSFP MSA Figure11-5 enables multi-level signaling to provide direct signal control in both directions. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.

The LPWn/PRSn signal operates in 3 voltage zones to indicate the state of Low Power mode for the module and Module Present for the host. Figure 12 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_PRSn signal and the module uses a voltage reference at 1.25V to determine the state of the M_LPWn signal.

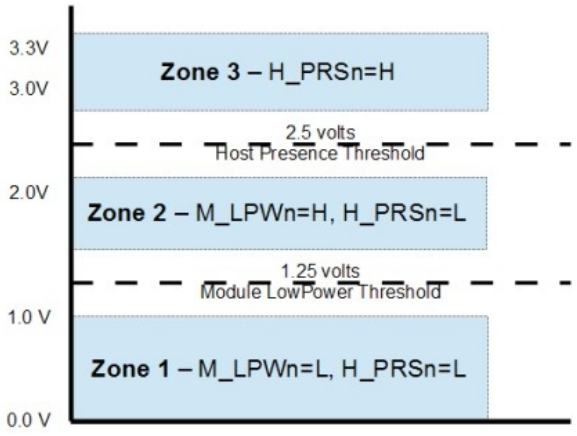

Figure 12: LPWn/PRSn Voltage Zones

The control interface and memory map of the OSFP module is compliant with the OSFP MSA. The OSFP module support I2C interface protocol defined by the OSFP MSA. Access clock frequency support a minimum of 100 kHz with no clock stretching and burst read/write of at least 32 bytes.

The module meets the following requirements:

1. The module initialize in hardware mode when LPWn is de-asserted.
2. The transmitter is disabled when the module is held in reset.
3. Tx Squelch function is implemented as defined by the OSFP MSA. When squelched, the transmitter remains on with the modulation turned off.
4. Rx Squelch function is implemented as defined by the OSFP MSA. When Rx CDR LOS is asserted,

CDR output is squelched.

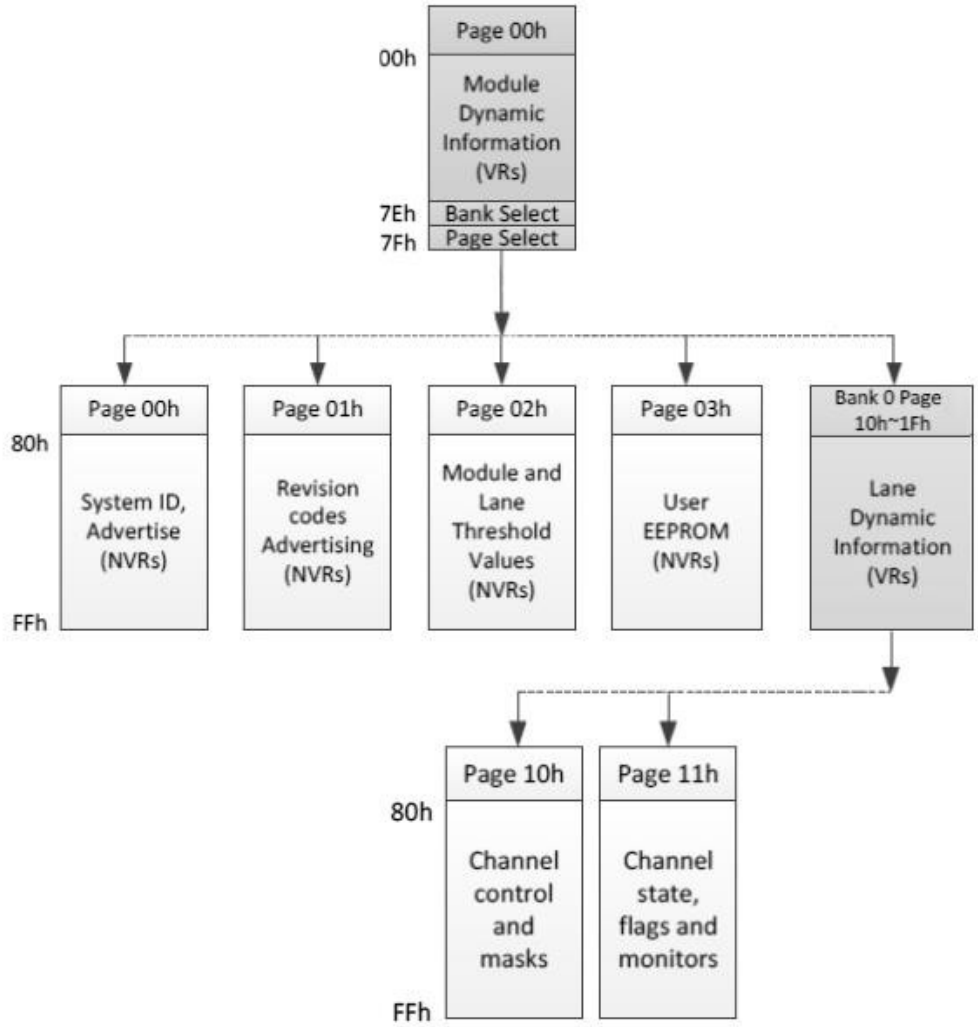

Figure 13: Simplified OSFP CMIS Module Memory Map Architecture

Revision History

Revision	Initiated	Reviewed	Approved	Revision History	Release Date
V1.a	Zaki	Eliss	Erik	Released.	Sep 18, 2023
V1.b	Viny/Julian	William/Eliss/Zaki	Erik	Update Figure 8, 9 and 10.	Nov 22, 2023

Quality

Eoptolink Technology has passed many quality system verifications, established an internationally standardized quality assurance system and strictly implemented standardized management and control in the course of design, development, production, installation and service. For latest certification/accreditation numbers, please, contact us.

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