Product Description

Do-Networks's QSFP-DD 8x100Gbps transceiver module can be used for 800 Gigabit Ethernet connections over 500m of single-mode fiber. The module includes eight parallel channels with a central wavelength of 1310nm, and the operating rate of each channel is 106.25Gbps. These 8-channel PAM4 parallel optical signals can be converted into 8-channel PAM4 electrical output signals; and there are 8 independent electrical input/output channels, which can convert PAM4 electrical input data into 8-channel PAM4 parallel optical signal. The transmitter of the module includes a bi-directional PAM4 re-timer ASIC with an 8-channel modulator driver and 8 EML Lasers. The receiver uses 8 photodiodes and integrated TIA, as well as the PAM4 re-timer. The electrical interface of the module is compliant with the 800GAUI-8 interface as defined by IEEE 802.3ck, and compliant with QSFP-DD MSA.

Features

- Supports 850Gbps
- Single 3.3V Power Supply
- Up to 500m over SMF with KP4 FEC supported at the Host side
- Dual MPO-12 connector
- 8x106.25Gbps (PAM4) electrical interface
- Driver and TIA integrated in the DSP at transmitter and receiver side
- Power dissipation < 14.5W
- Case temperature range: 0°C to 70°C (commercial)
- Safety Certification: TUV/UL/FDA*1
- RoHS Compliant

Applications*1

- 8x100G Ethernet
- 2x400G Ethernet
- 1x800G Ethernet

Ordering Information

Part No.	Data Rate	Fiber	Distance*2	Interface	Temp.	DDMI	CMIS
800G-QSFP-DD 2xDR4	850Gbps	SMF	500m	Dual MPO-12	0~70°C	Yes	CMIS5.0*3

*1: For more details, please contact with Do-Networks.
*2: Over G.652 SMF.
*3: CMIS5.0 or later version.

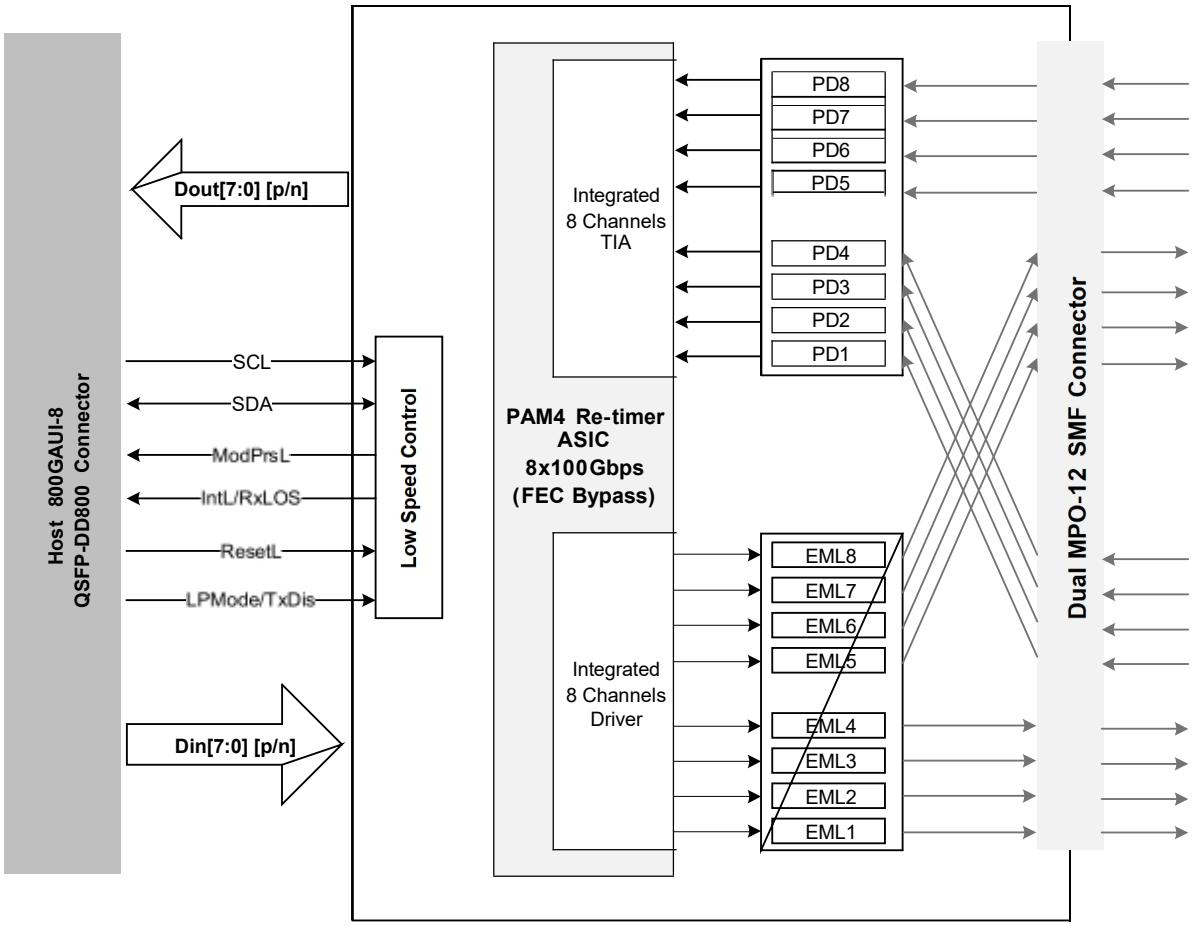

Figure 1: Transceiver Block Diagram

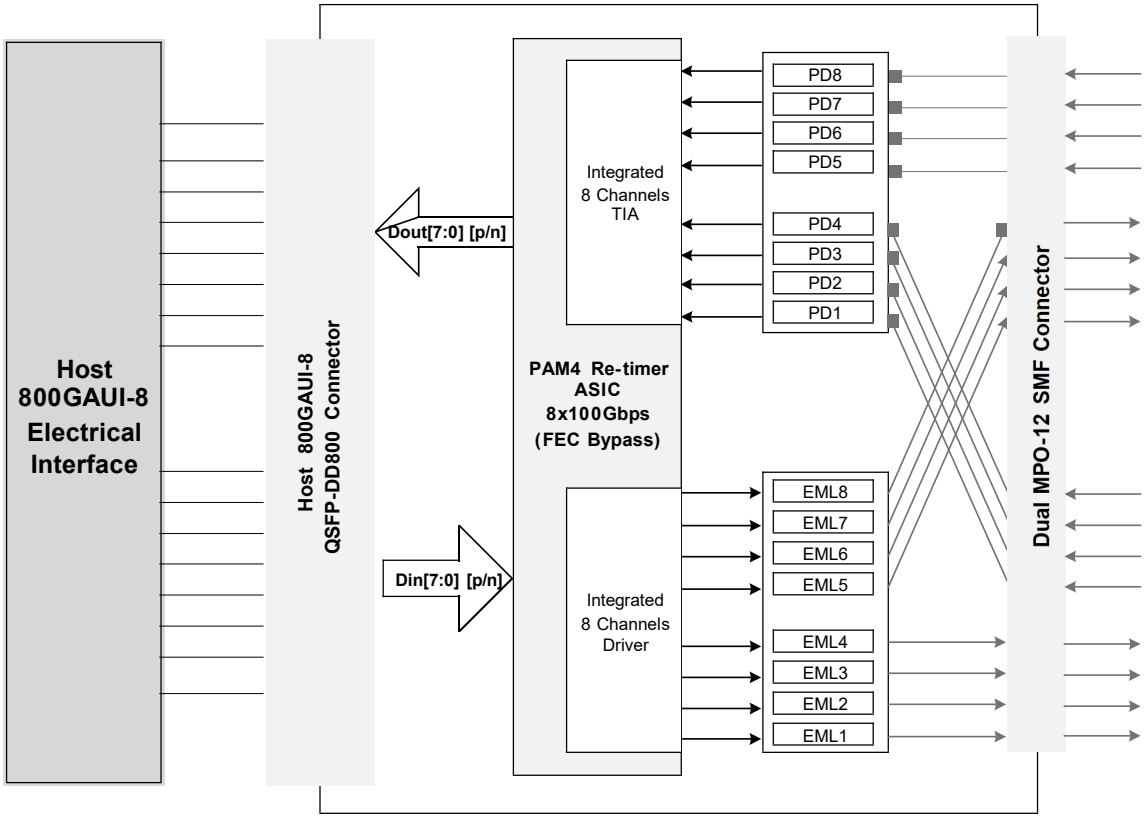

Figure 2: Application Reference Diagram

Transmitter

As shown in Figure 1, the transmitter path of the transceiver contains an 8x100Gbps 800GAUI-8 electrical input with Equalization (EQ) block, integrated electrical multiplexer, integrated EML driver, diagnostic monitors and 8 single mode EML lasers. The integrated electrical multiplexer and integrated EML driver converts 8 channels of 100 Gbps (PAM4) electrical input data to 8 channels of 100Gbps (PAM4) parallel optical signals. The transmitter complies with EN 60825 and CDRH Class 1 human eye safety compliance.

Receiver

As shown in Figure 1, the receiver path of the transceiver contains eight PIN photodiodes, integrated trans-impedance amplifiers (TIA), integrated de-multiplexer and 8x100G 800GAUI-8 compliant electrical output blocks. The PIN, integrated TIA and de-multiplexer converts 8 channels of 100Gbps (PAM4) parallel optical signals to 8 channels of 100Gbps (PAM4) electrical output data.

High Speed Electrical Signal Interface

The Application Reference Diagram shown in Figure2 illustrated the interface between the QSFP-DD module and Host 800GAUI-8. The high speed signal lines are internally AC-coupled and the electrical inputs are internally terminated to 100 Ohms differential. All transmitter and receiver electrical channels are compliant to module 800GAUI-8 specifications per IEEE 802.3ck.

Control Signal Interface

The ModPrsL, IntL/RxLOS, ResetL, LPMode/TxDis are the low speed signals for control and status. In addition, there is an industry standard two wire serial interface scaled for 3.3V LVTTL. It is implemented as a slave device. Signal and timing characteristics are further defined in the Control Interface& Memory map sections.
The registers of the serial interface memory are defined in the Control Interface & Memory map section.

Handling and Cleaning

The transceiver module may be damaged immediately due to current surge and overvoltage; Observe the precautions for normal operation of electrostatic discharge sensitive equipment; Attention shall also be paid to limiting transceiver module exposure to conditions beyond those specified in the absolute maximum ratings.
Optical connectors include female connectors. These elements will be exposed as long as the cable or port plug is not inserted. At this time, always pay attention to protection.
Each module is equipped with a port guard plug to protect the optical port. The protective plug shall always be in place whenever the optical fiber is not inserted. Before inserting the optical fiber, it is recommended to clean the end of the optical fiber connector to avoid contamination of the module optical port due to dirty connector. If contamination occurs, use standard MPO port cleaning methods.

Absolute Maximum Ratings

Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operating Conditions. It should not be assumed that limiting values of more than one parameter can be applied to the module concurrently. Exposure to any of the Absolute Maximum Ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage Temperature	Ts	-40		85	°C
3.3 V Power Supply Voltage	Vcc	-0.5	3.3	3.6	V
Data Input Voltage – Single Ended		-0.5		Vcc+0.5	V
Data Input Voltage – Differential*4				0.8	V
Relative Humidity	RH	5		85	%

*4：This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry. The damage threshold of the module input shall be at least 1600 mV peak to peak differential .

Recommended Operating Conditions*5

Recommended Operating Conditions specify parameters for which the optical and electrical characteristics hold unless otherwise noted. Optical and electrical characteristics are not defined for operation outside the Recommended Operating Conditions, reliability is not implied and damage to the module may occur for such operation over an extended period of time.

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating case temperature*6	Tc	0		70	°C
Power supply voltage	Vcc	3.135	3.3	3.465	V
Power dissipation	P_D			14.5	W
Electrical Signal Rate per Channel (PAM encoded)*7			53.125		GBd
Optical Signal Rate per Channel (PAM encoded)*8			53.125		GBd
Power Supply Noise*9				66	mVpp
Receiver Differential Data Output Load		100			Ohm
Fiber Length (9μm SMF)*10				500	m

*5: Power Supply specifications, Instantaneous, sustained and steady state current compliant with QSFP-DD MSA Power Classification.

*6: The position of case temperature measurement is shown in Figure 9.

*7: 800GAUI-8 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.

*8: 8×100G-DR operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.

*9: Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 7 for recommended power supply filter.

*10: 9μm SMF. The maximum link distance is based on an allocation of 1dB of attenuation and 3dB total connection and

splice loss. The loss of a single connection shall not exceed 0.5dB.

General Electrical Characteristics*11

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Symbol	Min.	Typical	Max.	Unit
Transceiver Power Consumption			13.5	14.5	W
Transceiver Power Supply Current, Total			4310	4630	mA
AC coupling capacitors (Internal)			0.1		µF

*11: For control signal timing including ModSelL, ResetL, LPMode/TxDisable, ModePrsL, IntL/RxLOSL, SCL and SDA see Control Interface Section.

Reference Points

Test Point	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are made between TP1 and TP4 as illustrated in Figure 3.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 802.3ck 162.9.3 and 162.9.4. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided in 802.3ck 162.9.3.2
TP2	Unless specified otherwise, all transmitter measurements defined in 802.3ck 162.9.3 are made at TP2 utilizing the test fixture specified in Annex 162B.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 802.3ck 162.9.4 are made at TP3 utilizing the test fixture specified in Annex 162B.

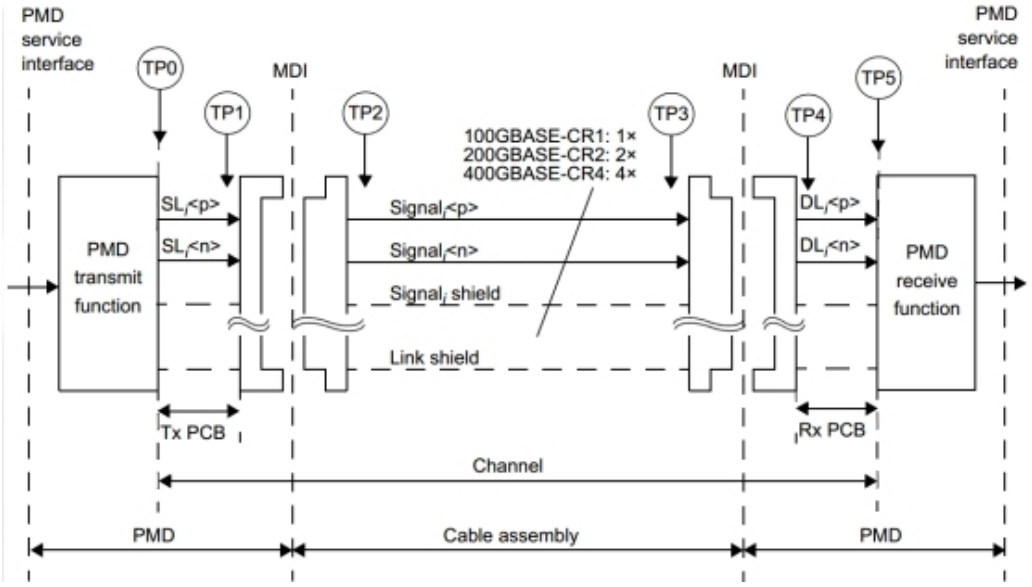

Figure 3: IEEE 802.3ck 100GBASE-CR1, 200GBASE-CR2 or 400GBASE-CR4 link

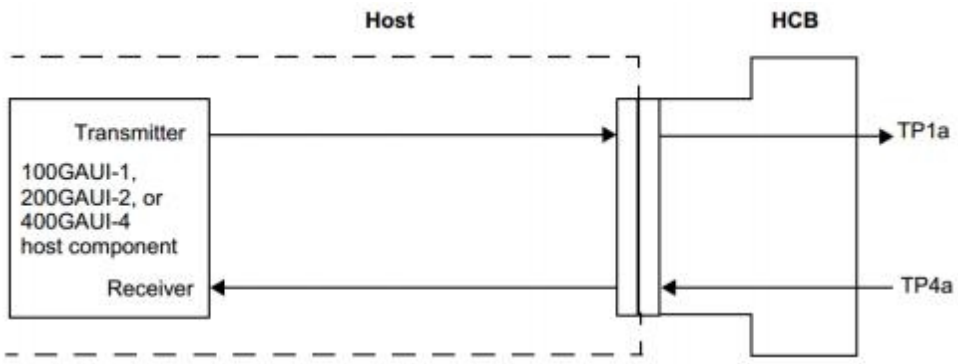

Figure 4: IEEE 802.3ck host compliance points TP1a, TP4a

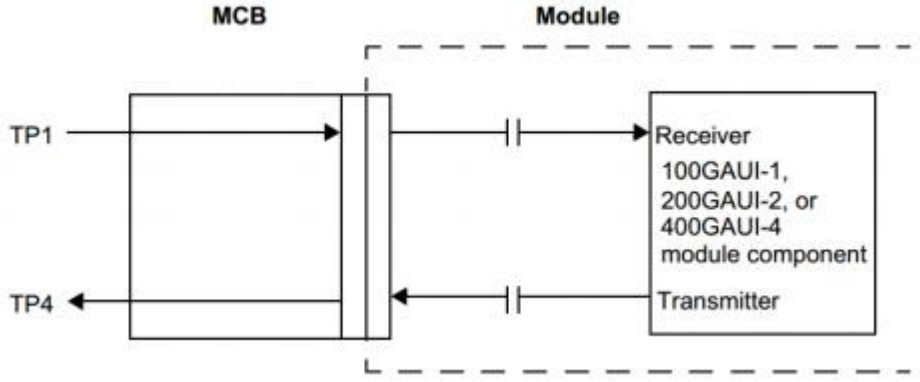

Figure 5: IEEE 802.3ck module compliance points TP1, TP4

High Speed Electrical Input Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point	Min.	Typical	Max.	Unit	Conditions
Signaling Rate, Per Lane (PAM4 encoded)	TP1		53.125		GBd	+/- 100 ppm
Differential peak-peak Input Voltage Tolerance	TP1a	750			mV	
AC common-mode RMS voltage tolerance	TP1a	25			mV	
Differential-mode to common-mode return loss	TP1	Equation (120G–2)			dB	802.3ck
Effective return loss, ERL	TP1	8.5			dB	
Differential termination mismatch	TP1			10	%	
Module stressed input tolerance	TP1a		See 120G.3.4.3			802.3ck
Single-ended voltage tolerance range	TP1a	-0.4		3.3	V	
DC common-mode voltage tolerance range	TP1	-350		2850	mV	
Module stressed input tolerance test :						

Pattern generator transition time		9	ps	
Applied peak-peak sinusoidal jitter		Table 162-16		802.3ck
Eye height		10	mV	
Vertical eye closure, VEC	12		12.5 dB	
Crosstalk differential peak-to-peak voltage		845	mV	
Crosstalk transition time		8.5	ps	

High Speed Electrical Output Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point	Min.	Typical	Max.	Unit
Signaling Rate, Per Lane (range)	TP4		53.125*12 ± 100 ppm		GBd
AC common-mode output voltage	TP4			25	mV
Differential peak-to-peak input voltage Short mode Long mode	TP4			600 845	mV
Eye height	TP4	15			mV
Vertical eye closure	TP4			12	dB
Effective return loss	TP4	8.5			dB
Common-mode to differential-mode return loss	TP4	Equation (120G– 1)			dB
Differential termination mismatch	TP4			10	%
Transition time	TP4	8.5			ps
DC common-mode voltage tolerance	TP4	-0.35		2.85	V

*12: The signaling rate range is derived from the PMD receiver input.

High Speed Optical Transmitter Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Optical Characteristics @TP2 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling speed per lane			106.25		Gbps
Modulation format			PAM4		
Center wavelength	λ	1304.5	1311	1317.5	nm
Side-mode Suppression Ratio	SMSR	30			dB
Extinction ratio	ER	3.5			dB

Average launch power[*13]	-2.9	4	dBm
OMA_{outer} per lane	-0.8	4.2	dBm
Launch power in OMA_{outer} minus TDECQ, each lane:	-2.2		dBm
TDECQ (PAM4)		3.4	dB
$RIN_{21.4}$ OMA		-136	dB/Hz
Average launch power of OFF transmitter		-15	dBm
Optical return loss tolerance		21.4	dB
Transmitter Reflectance		-26	dB

*13: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

High Speed Optical Receiver Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Optical Characteristics @TP3 Test Point

Parameter	Symbol	Min	Typical	Max	Unit
Signaling speed per lane			106.25		Gbps
Center wavelength	λ	1305.5	1311	1317.5	nm
Damage threshold		5			dBm
Average receiver power per lane		-5.9		4	dBm
Saturation receive power (OMA_{outer}) per Lane				4.2	dBm
Unstressed Receiver Sensitivity (OMA) Per Lane	Sen[*14]			-4.4	dBm
Stressed receiver sensitivity(OMA_{outer}), each lane				-1.9	dBm
Conditions of stressed receiver sensitivity test[*15]:					
Stressed eye closure for PAM4 (SECQ), lane under test				3.4	dB
OMA_{outer} of each aggressor lane				4.2	dBm
LOS Assert (Avg.)	LOSA	-15			dBm
LOS De-Assert (Avg.)	LOSD			-10	dBm
RSSI accuracy		-2		+2	dB
Receiver reflectance				-26	dB

*14: Measured with conformance test signal at TP3 for the BER specified in IEEE Std 802.3cd clause 140.1.1.

*15: These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Regulatory & Compliance Issues

Various standard and regulations apply to the 800G-QSFP-DD 2xDR4 modules. These include eye-safety, Component Recognition, RoHS, ESD, EMC and Immunity. Please note the transmitter module is a Class 1 laser product. See Regulatory Compliance Table for details.

Regulatory Compliance Table

Feature	Test Method	Performance
Laser Eye Safety and Equipment Type Testing 	(IEC) EN 62368-1:2014+A11 (IEC) EN 60825-1:2014 (IEC) EN 60825-2:2004+A1+A2	CDRH Accession Number:2132182-000 TUV File: R 50457725 0001 CB File: JPTUV-100513
Component Recognition	Underwriters Laboratories (UL) and Canadian Standards Association (CSA) Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File: E317337
RoHS Compliance	RoHS Directive 2011/65/EU&(EU)2015/863	Less than 100 ppm of cadmium. Less than 1000 ppm lead, mercury, hexavalent chromium, poly brominated biphenyls (PPB) , poly brominated biphenyl ethers (PBDE), dibutyl phthalate, butyl benzyl phthalate, bis (2-ethylhexyl) phthalate and diisobutyl phthalates.
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM)	High speed contacts shall withstand 1000V. All other contacts shall withstand 2000 V.
Electrostatic Discharge (ESD) to the Optical Connector Receptacle	IEC 61000-4-2:2008	When installed in a properly grounded housing and chassis the units are subjected to 15kV air discharges during operation and 8kV direct discharges to the case.
Electromagnetic Interference (EMI)	FCC Part 15 Class B; CISPR 32 (EN55032) 2015;	System margins are dependent on customer board and chassis design.
Immunity	IEC 61000-4-3:2010; EN55035:2017	Typically shows no measurable effect from a 10V/m field swept from 80 MHz to 6 GHz applied to the module without a chassis enclosure.

Electrostatic Discharge (ESD)

800G-QSFP-DD 2xDR4 complies with the ESD requirements described in the Regulatory Compliance Table. However, in the normal processing and operation of optical transceiver, the following two types of situations need special attention.

Case I: Before inserting the transceiver into the rack meeting the requirements of QSFP-DD MSA, ESD preventive measures must be taken to protect the equipment. For example, the grounding wrist strap, workbench and floor should be used wherever the transceiver is handled.

Case II: After the transceiver is installed, the electrostatic discharge outside the chassis of the host equipment shall be within the scope of system level ESD requirements. If the optical interface of the transceiver is exposed outside the host equipment cabinet, the transceiver may be subject to equipment system level ESD requirements.

Electromagnetic Interference (EMI)

Communication equipment with optical transceivers is usually regulated by FCC in the United States and CENELEC EN55032 (CISPR 32) in Europe. The compliance of 800G-QSFP-DD 2xDR4 with these standards is detailed in the regulatory compliance table. The metal shell and shielding design of 800G-QSFP-DD 2xDR4 will help equipment designers minimize the equipment level EMI challenges they face.

Flammability

800G-QSFP-DD 2xDR4 optical transceiver meets UL certification requirements, its constituent materials have heat and corrosion resistance, and the plastic parts meet UL94V-0 requirements.

QSFP-DD Transceiver Electrical Pad Layout

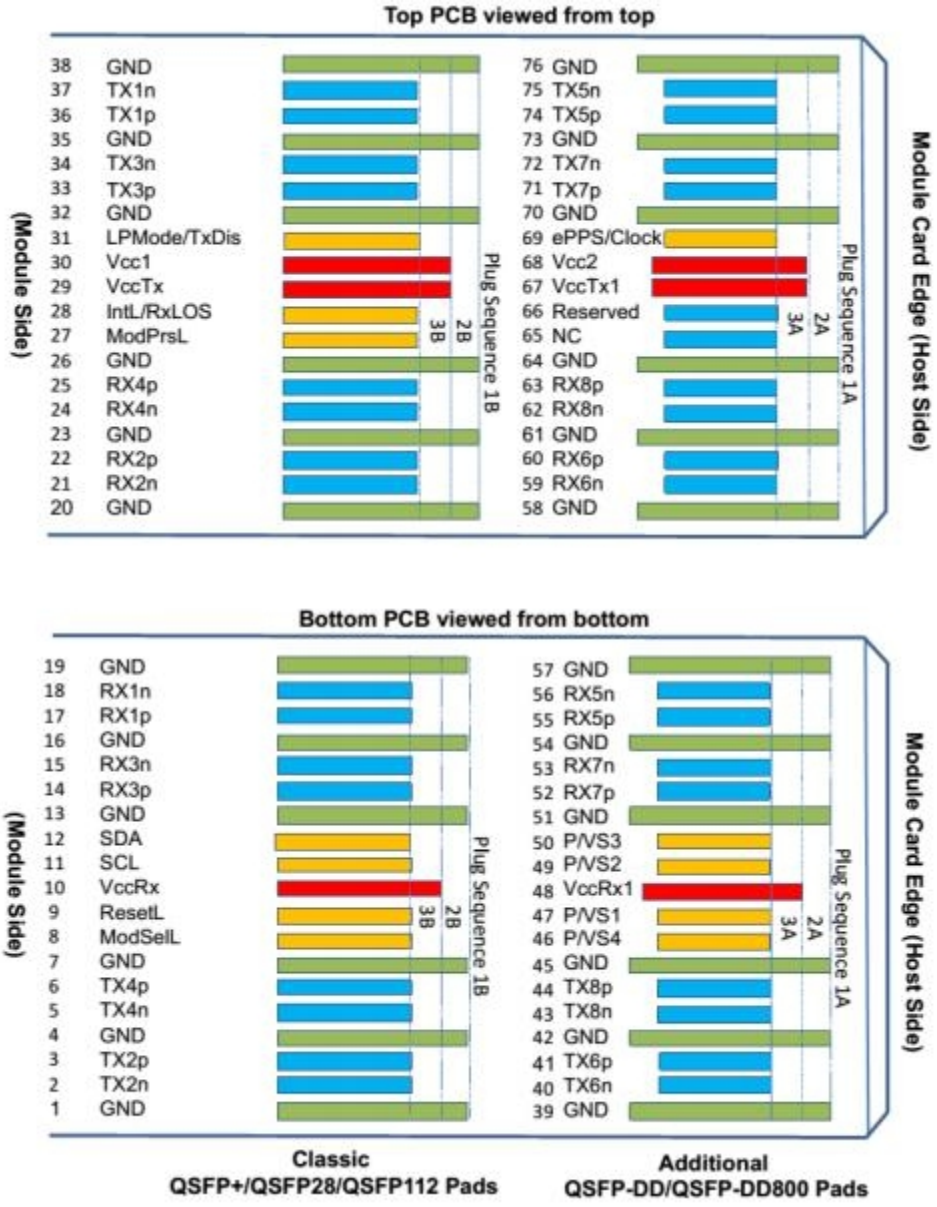

Figure 6: QSFP-DD Module Pinout

Pin Arrangement and Definition

Pin	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL /RxLOS	Interrupt/ optional RxLOS	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode/ TxDIS	Low Power mode/optional TX Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	

38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46	LVCMOS/ CML-I	P/ VS4	Programmable/ Module Vendor Specific 4	3A	5
47	LVCMOS/ CML-I	P/ VS1	Programmable/ Module Vendor Specific 1	3A	5
48		VccRx1	3.3V Power Supply	2A	2
49	LVCMOS/ CML-O	P/ VS2	Programmable/ Module Vendor Specific 2	3A	5
50	LVCMOS/ CMLO	P/ VS3	Programmable/ Module Vendor Specific 3	3A	5
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LV-CMOS -I	ePPS/Clo ck	1 PPS PTP clock or reference clock input	3A	6
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1500 mA.

3: Reserved and No Connect pins may be terminated with 10k ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 k Ohms and less than 100 pF.

4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

5: Full definitions of the P/VSx signals currently under development. On new designs not used P/VSx signals are recommended to be terminated on the host with 10k ohms .

6: The ePPS/Clock pin is pulled down to ground with 10km ohms on the module.

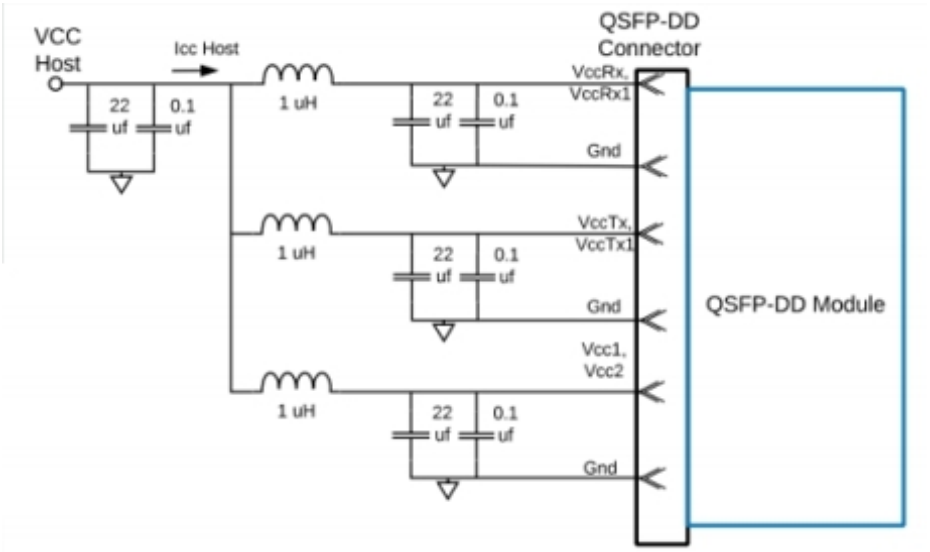

Figure 7: Host Board Power Supply Filter

During power transient events, the host should ensure that any neighboring modules sharing the same supply stay within their specified supply voltage limits. The host should also ensure that the intrinsic noise of the power rail is filtered in order to guarantee the correct operation of the optical modules. The reference power supply filter is shown in Figure 7.

Package Outline

The module is designed to meet the package outline defined in the QSFP-DD MSA specification. See the package outline for details.

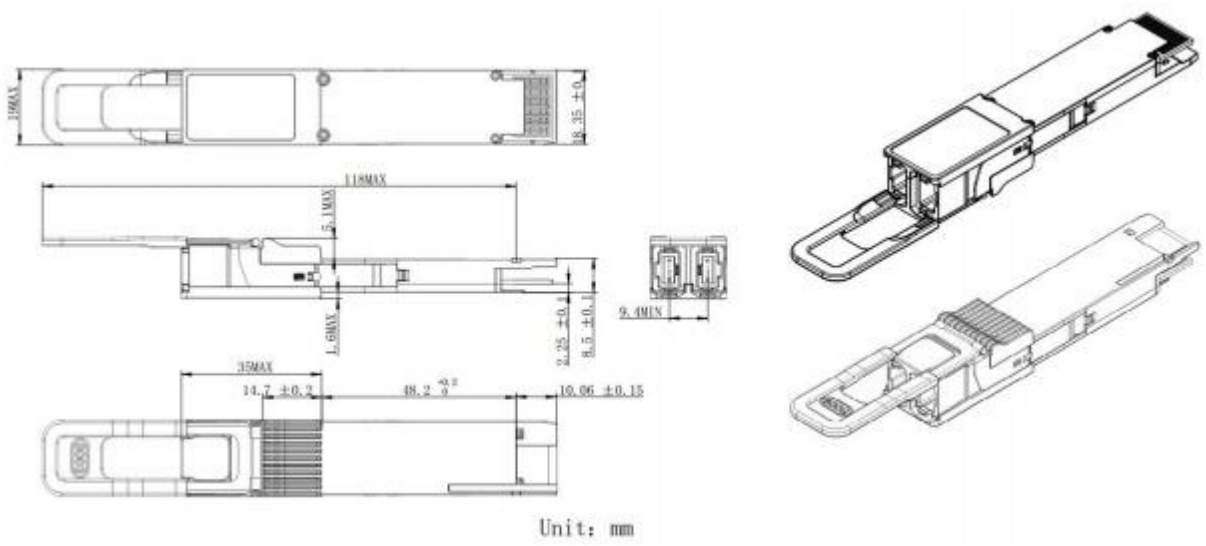

Figure 8: Mechanical Package Outline (All dimensions in mm)

*This 2D drawing is only for reference, please check with Do-Networks before ordering.

The bellow picture shows the location of the hottest spot for measuring module case temperature. In addition, the digital diagnostic monitors (DDM) temperature is also calibrated to this spot.

TBD

Figure 9: Case Temperature Measurement Point (All dimensions in mm)

The optical interface port is a male Dual MPO-12 connector. Mates with two standard type MPO-12 female plug connectors with down-angled interface.

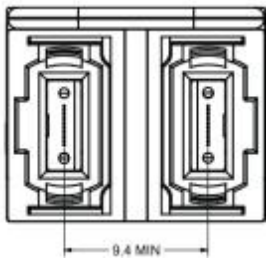

Figure 10: Module Optical Interface (looking into the optical port)

Control Interface & Memory Map

The control interface combines dedicated signal lines for ModeSelL, ResetL, LPMode/TxDis, ModPrsL, IntL/RxLOS with two-wire serial (TWS), interface clock (SCL) and data (SDA), signals to provide users rich functionality over an efficient and easily used interface.

SCL and SDA

The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre- charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

ModSelL

The ModSelL is an input signal that shall be pulled to Vcc in the QSFP-DD modules. When held low by the host, the module responds to TWI serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single TWI interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any TWI interface communication from the host.

In order to avoid conflicts, the host system shall not attempt TWI interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state.

LPMode/TxDis

LPMode/TxDis is a dual-mode input signal from the host operating with active high logic. It shall be pulled towards Vcc in the module. At power-up or after ResetL is deasserted LPMode/TxDis behaves as LPMode. If supported, LPMode/TxDis can be configured as TxDis using the TWI interface except during the execution of a reset. LPMode is used in the control of the module power mode.

When LPMode/TxDis is configured as LPMode, the module behaves as though TxDis=0. By using the LPMode signal and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits the host controls how much power a module can consume. When LPMode/TxDis is configured as TxDis, the module behaves as though LPMode=0.

Changing LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is high disables all optical transmitters. If the module was in low power mode, then the module transitions out of low power mode at the same time. If the module is already in high power state (Power Override control bits) with transmitters already enabled, the module shall disable all optical transmitters. Changing the LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is low, simply changes the

behavior of the mode of LPMode/TxDis. The behavior of the module depends on the Power Override control bits.

ModPrsL

ModPrsL shall be pulled up to Vcc Host on the host board and pulled low in the module. The ModPrsL is asserted "Low" when the module is inserted. The ModPrsL is deasserted "High" when the module is physically absent from the host connector due to the pull-up resistor on the host board.

IntL/RxLOSL

IntL/RxLOSL is a dual-mode active-low, open-collector output signal from the module. It shall be pulled up towards Vcc on the host board. At power-up or after ResetL is released to high, IntL/RxLOSL is configured as IntL. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the TWI serial interface. The IntL signal is deasserted "High" after all set interrupt flags are read. If dual mode operation supported, IntL/RxLOSL can be optionally programmed as RxLOSL using the TWI interface except during the execution of a reset. If the module has no interrupt flags asserted (IntL/RxLOSL is high), there should be no change in IntL/RxLOSL states after the mode change.
If IntL/RxLOSL is configured as RxLOSL, a low indicates that there is a loss of received optical power on at least one lane. "high" indicates that there is no loss of received optical power. The actual condition of loss of optical receive power is specified by other governing documents, as the alarm threshold level is application specific. The module shall pull RxLOSL to low if any lane in a multiple lane module or cable has a LOS condition and shall release RxLOSL to high only if no lane has a LOS condition.

Low Speed Control and Sense Signals

Parameter	Symbol	Min.	Typical	Max.	Unit
SCL and SDA	VOL	0		0.4	V
	VOH	V_{CC}-0.5		V_{CC}+0.3	V
SCL and SDA	VIL	-0.3		V_{CC}*0.3	V
	VIH	V_{CC}*0.7		V_{CC}+0.5	V
LPMode/TxDis, ResetL, ModSelL	VIL	-0.3		0.8	V
	VIH	2		V_{CC}+0.3	V
LPMode, ResetL, ModSelL	|Iin|			360	μA
IntL/RxLOSL	VOL	0		0.4	V
	VOH	V_{CC}-0.5		V_{CC}+0.3	V
ModPrsL	VOL	0		0.4	V

Memory Map

The control interface and memory map of the QSFP-DD module is compliant with the QSFP-DD MSA. The QSFP-DD module support I2C interface protocol defined by the QSFP-DD MSA. Access clock frequency support a minimum of 100 kHz with no clock stretching and burst read/write of at least 32 bytes. The module meets the following requirements:

1. The module initialize in hardware mode when LPMode is de-asserted.
2. The transmitter is disabled when the module is held in reset.
3. Tx Squelch function is implemented as defined by the QSFP-DD MSA. When squelched, the transmitter remains on with the modulation turned off.
4. Rx Squelch function is implemented as defined by the QSFP-DD MSA. When Rx CDR LOS is asserted, CDR output is squelched.

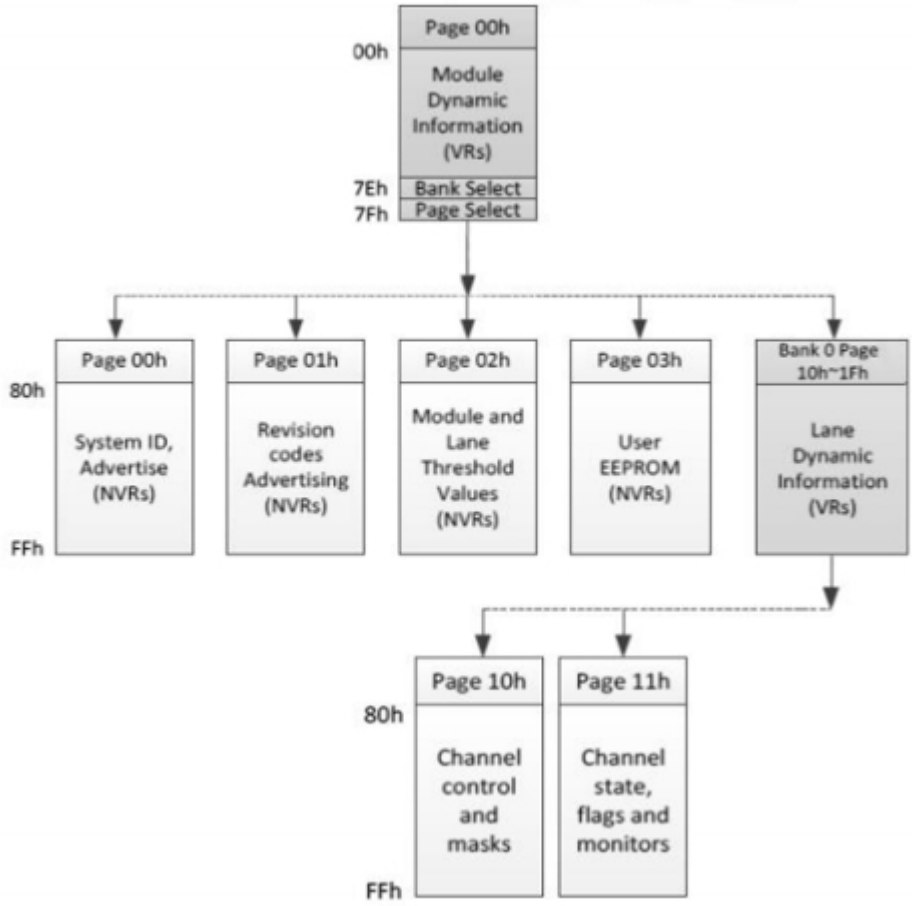

Figure 11: Simplified QSFP-DD CMIS Module Memory Map Architecture

Revision History

Revision	Initiated	Reviewed	Approved	Revision History	Release Date
V1.a	Zaki	Eliss/Viny	Erik	Preliminary.	Apr 25, 2023
V1.b	Viny	Eliss	Erik	Released.	Aug 16, 2023
V1.c	Angela	William/Lucker/Zaki	Erik	Update the figure 8, figure 10.	Jan 09, 2024

Quality

Do-Networks Technology has passed many quality system verifications, established an internationally standardized quality assurance system and strictly implemented standardized management and control in the course of design, development, production, installation and service. For latest certification/accreditation numbers, please, contact us.

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