Product Description

Do-Networks's OSFP transceiver module is designed for use in 800 Gigabit Ethernet links over 2km single mode fiber. The module has 8 independent electrical input/output channels operating up to 106.25Gbps per channel. This transceiver consists of two transmitter/receiver units, with each operating on a set of 4 wavelengths on the ITU G.694.2 CWDM grid near 1300nm. The transmitter path of the module incorporates a bi-directional PAM4 re-timer ASIC integrated with an 8-channels high swing modulator driver, 8-channels PIC with CWDM MUX integrated and 4 CWDM CW lasers. On the receiver path, two optical AWG are coupled to 8 photodiodes and integrated TIA, along with the PAM4 re-timer. The electrical interface of the module is compliant with the 800GAUI-8 interface as defined by IEEE 802.3ck, and compliant with OSFP MSA.

Features

- Supports 850Gbps
- Single 3.3V Power Supply
- Up to 2km over SMF with KP4 FEC supported at the Host side
- Dual Duplex LC connector
- 8x106.25Gbps (PAM4) electrical interface
- Sipho based transmitter
- Driver and TIA integrated in the DSP at transmitter
- Power dissipation < 15W
- Case temperature range: 0°C to 70°C (commercial)
- Safety Certification: TUV/UL/FDA*1
- RoHS Compliant

Applications*1

- 1x800G Ethernet

Part No.	Data Rate	Fiber	Distance*2	Interface	Temp.	DDMI	CMIS
800G-OSFP112-2xFR4	850Gbps	SMF	2km	Dual LC	0~70°C	Yes	CMIS5.0*4

1: For more details, please contact with Do-Networks.
*2: Over G.652 SMF.
*3: Based on Broadcom DSP.

*4: CMIS5.0 or later version.

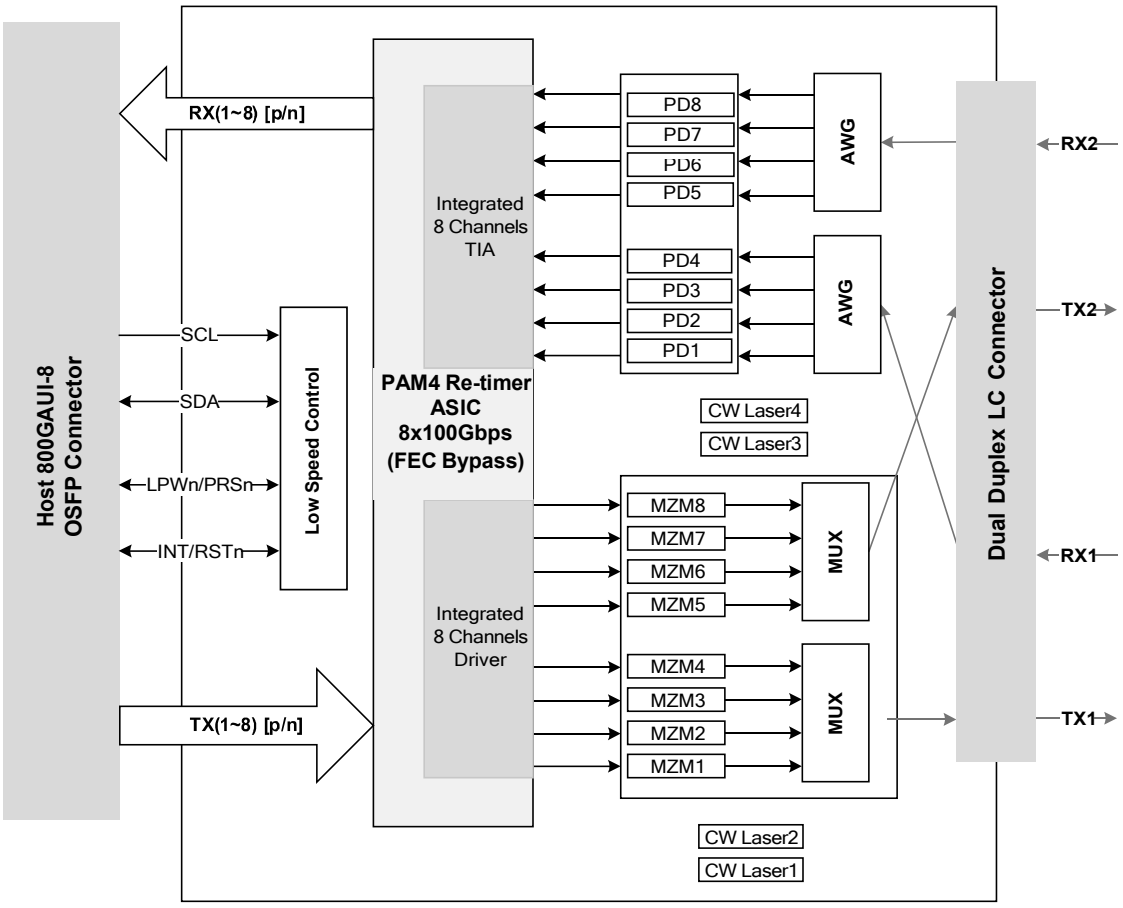

Figure 1: Transceiver Block Diagram

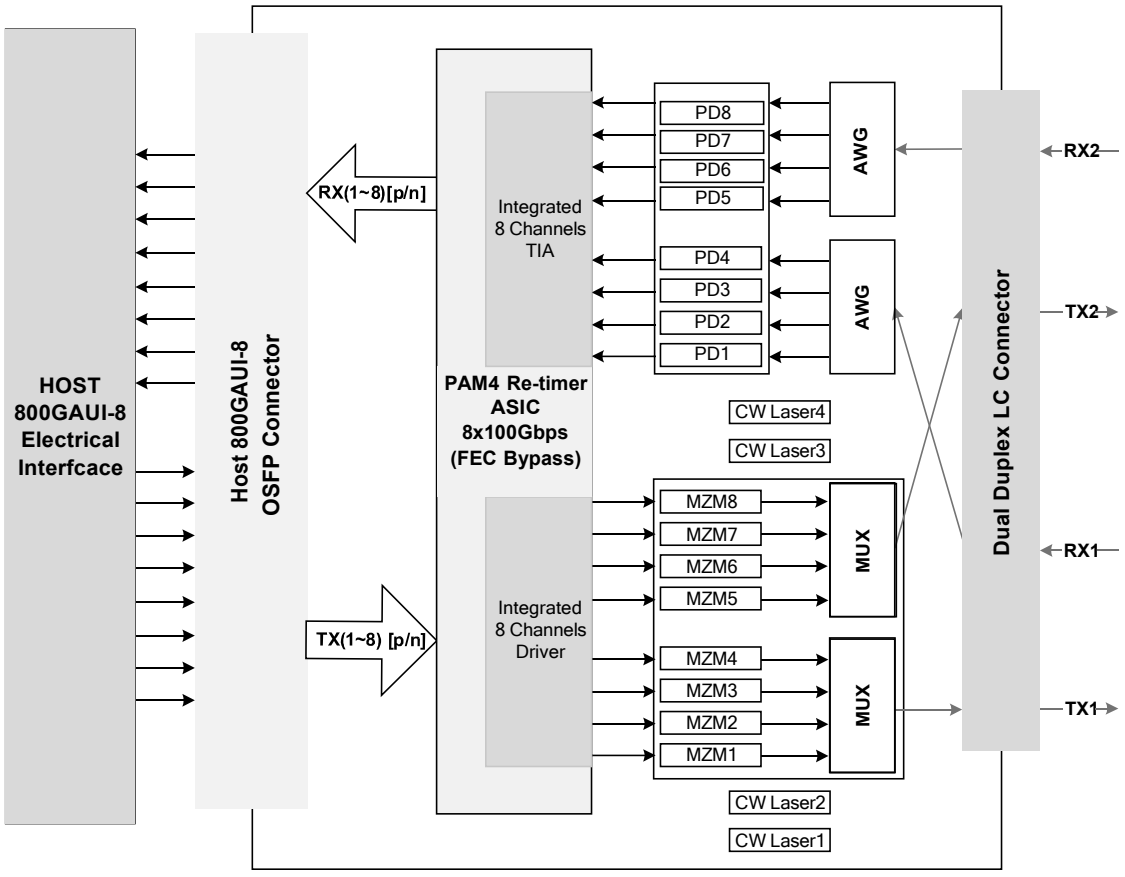

Figure 2: Application Reference Diagram

Transmitter

As shown in Figure 1, the transmitter path of the transceiver contains an 8x100Gbps 800GAUI-8 electrical input with Equalization (EQ) block, integrated retimer with high swing output, diagnostic monitors, single sipho PIC with 8 independent MZM modulator and 2 CWDM MUX and 4 CW CWDM lasers. The integrated electrical retimer converts 8 channels of 100 Gbps (PAM4) electrical input data to 8 channels of 100Gbps (PAM4) high output swing optical signals. The sipho PIC modulate 8 channels of optical signal and transfer to 2 optical port. The transmitter complies with EN 60825 and CDRH Class 1 human eye safety compliance.

Receiver

As shown in Figure 1, the receiver path of the transceiver contains optical AWG, eight PIN photodiodes, integrated trans-impedance amplifiers (TIA), and 8x100G 800GAUI-8 compliant electrical output blocks. The PIN, AWG, integrated TIA and retimer converts 8 channels of 100Gbps (PAM4) parallel optical signals to 8 channels of 100Gbps (PAM4) electrical output data.

High Speed Electrical Signal Interface

The interface between the OSFP module and an ASIC/SerDes and is shown in Figure 2. The highspeed signal lines are internally AC-coupled and the electrical inputs are internally terminated to 100 Ohms differential. All transmitter and receiver electrical channels are compliant to module 800GAUI-8 specifications per IEEE 802.3ck.

Control Signal Interface

The module has the following low speed signals for control and status: LPWn/PRSn, INT/RSTn. In addition, there is an industry standard two wire serial interface scaled for 3.3 volt LVTTL. It is implemented as a slave device. Signal and timing characteristics are further defined in the Control Characteristics and Control Interface& Memory Map sections.
The registers of the serial interface memory are defined in the Control Interface & Memory Map section.

Handling and Cleaning

Exposure to current surges and overvoltage events can cause immediate damage to the transceiver module. Observe the precautions for normal operation of electrostatic discharge sensitive equipment; Attention shall also be paid to limiting transceiver module exposure to conditions beyond those specified in the absolute maximum ratings. Optical connectors include female connectors. These elements will be exposed as long as the cable or port plug is not inserted. At this time, always pay attention to protection. Each module is equipped with a port guard plug to protect the optical port. The protective plug shall always be in place whenever the optical fiber is not inserted. Before inserting the optical fiber, it is recommended to clean the end of the optical fiber connector to avoid contamination of the module optical port due to dirty connector. If contamination occurs, use standard LC port cleaning methods.

Absolute Maximum Ratings

Exceeding the absolute maximum ratings table may cause permanent damage to the device. This is just an emphasized rating, and does not involve the functional operation of the device that exceeds the specifications of this technical specification under these or other conditions. Long-term operation under absolute maximum ratings will affect the reliability of the device.

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage Temperature	Ts	-40		85	°C
3.3 V Power Supply Voltage	Vcc	-0.5	3.3	3.6	V
Data Input Voltage – Single Ended		-0.5		Vcc+0.5	V
Data Input Voltage – Differential*5				0.8	V
Relative Humidity	RH	5		85	%

*5: This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry. The damage threshold of the module input shall be at least 1600 mV peak to peak differential.

Recommended Operating Conditions*6

For operations beyond the recommended operating conditions, optical and electrical characteristics are not defined, reliability is not implied, and such operations for a long time may damage the module.

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating case temperature*7	Tc	0		70	°C
Storage temperature	Ts	-40		+85	°C
Power supply voltage	Vcc	3.135	3.3	3.465	V
Power dissipation	P			15	W
In-rush, instantaneous peak current	I_Peak			6000	mA
In-rush and discharge current, dI/dt	I_Inrush			100	mA/us
Electrical Signal Rate per Channel (PAM encoded) *8			53.125		GBaud
Optical Signal Rate per Channel (PAM encoded) *9			53.125		GBaud
Power Supply Noise *10				66	mVpp
Fiber Length (9um SMF) *11				2	km

*6: Power Supply specifications, Instantaneous, sustained and steady state current compliant with OSFP MSA Power Classification.

*7: The position of case temperature measurement is shown in Figure 9.

*8: 800GAUI-8 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.

*9: 800G 2×FR4 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.

*10: Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 7 for recommended power supply filter.

*11: 9μm SMF. The maximum link distance is based on an allocation of 1dB of attenuation and 3dB total connection and

splice loss. The loss of a single connection shall not exceed 0.5dB.

General Electrical Characteristics*12

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Symbol	Min.	Typical	Max.	Unit
Transceiver Power Consumption				15	W
Transceiver Power Supply Current, Total				4550	mA
AC coupling capacitors (Internal)			0.1		uF

*12: For control signal timing including LPWn/PRSn, INT/RSTn, SCL and SDA see Control Interface Section.

Reference Points

Test Point	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are made between TP1 and TP4 as illustrated in Figure 3.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 802.3ck 162.9.3 and 162.9.4. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided in 802.3ck 162.9.3.2
TP2	Unless specified otherwise, all transmitter measurements defined in 802.3ck 162.9.3 are made at TP2 utilizing the test fixture specified in Annex 162B.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 802.3ck 162.9.4 are made at TP3 utilizing the test fixture specified in Annex 162B.

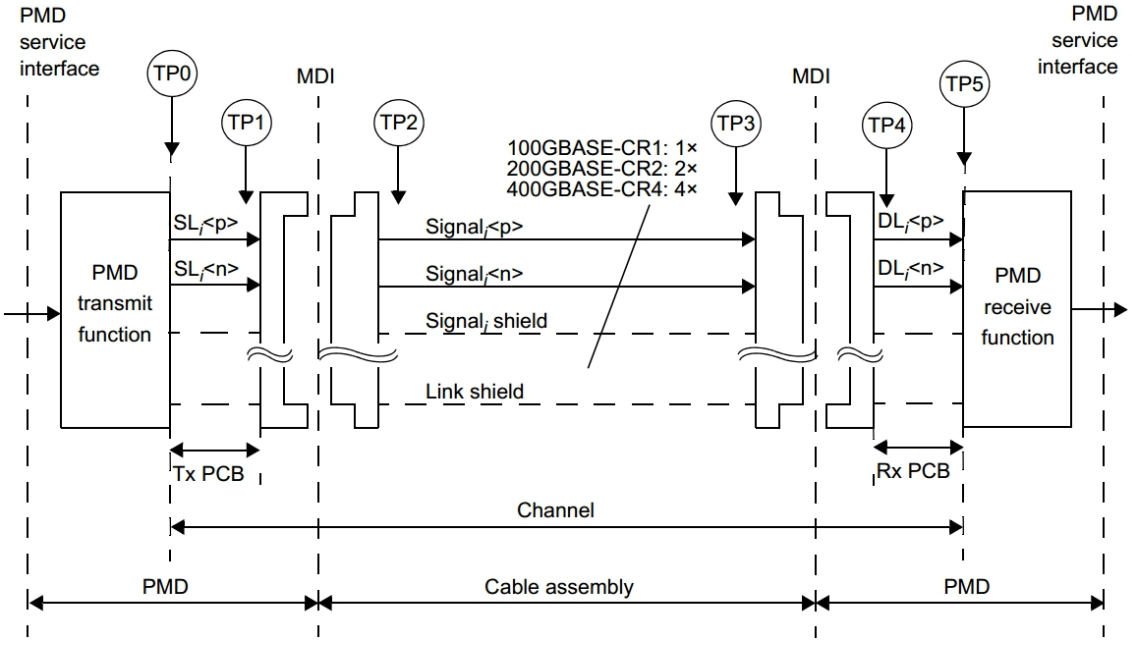

Figure 3: IEEE 802.3ck 100GBASE-CR1, 200GBASE-CR2 or 400GBASE-CR4 link

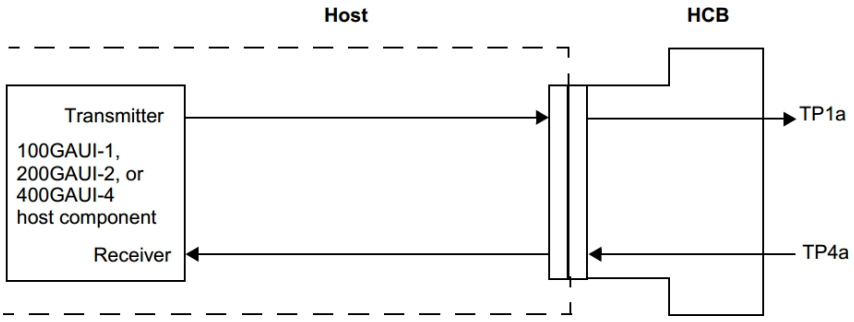

Figure 4: IEEE 802.3ck 400GAUI-4 compliance points TP1a, TP4a

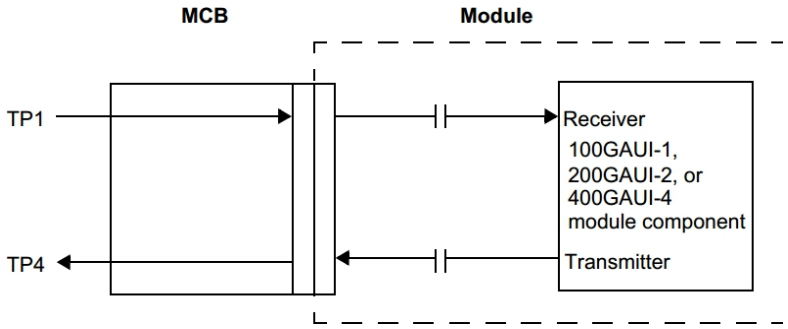

Figure 5: IEEE 802.3ck 400GAUI-4 compliance points TP1, TP4

High Speed Electrical Input Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Test Point	Min.	Typical	Max.	Unit	Conditions
Signaling Rate, Per Lane (PAM4 encoded)	TP1		53.125		GBd	+/- 100 ppm
Differential peak-peak Input Voltage Tolerance	TP1a	900			mV	
Effective Return Loss (min)	TP1		TBD		dB	802.3ck
Common mode to differential return loss (min)	TP1		TBD		dB	802.3ck
Differential Termination Mismatch	TP1			10	%	
Module stressed input test	TP1a					
Single-ended voltage tolerance range	TP1a	-0.4		3.3	V	
DC common-mode output voltage*13	TP1	-350		2850	mV	
Module stressed input test *14						
Eye width			TBD		UI	
Applied peak-peak sinusoidal jitter			Table 120G-7			802.3ck
Eye height			15		mV	

*13: DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

*14: Module stressed input tolerance is measured using the procedure defined in 120G.1.1.

High Speed Electrical Output Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Test Point	Min.	Typical	Max.	Unit
Signaling Rate, Per Lane (range)	TP4a		53.125 ± 100 ppm		GBd
Differential peak-to-peak input voltage tolerance	TP4			900	mV
Effective Return Loss	TP4a		TBD		dB
Common to differential mode conversion return loss (min)	TP4a		Equation (120G-1)		dB
Differential termination mismatch	TP4a			10	%
Host stressed input test	TP4		120G3.3.2		
Common mode voltage	TP4a	-0.35		2.85	V

High Speed Optical Transmitter Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Optical Characteristics @TP2 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling speed per lane			106.25		Gbps
Modulation format			PAM4		
Center wavelength	λc0	1264.5	1271	1277.5	nm
	λc1	1284.5	1291	1297.5	nm
	λc2	1305.25	1311	1317.5	nm
	λc3	1325.25	1331	1337.5	nm
Side-mode Suppression Ratio	SMSR	30			dB
Extinction ratio	ER	3.5			dB
Total average launch power				10.4	dBm
Average launch power*15		-3.2		4.4	dBm
OMA per lane for TDECQ<1.4dB for 1.4dB≤TDECQ≤3.4dB		-0.2 -1.6+TDECQ		3.7	dBm
Difference in launch power between any two lanes (OMA_{outer})				3.9	dB
Transmitter and dispersion eye closure quaternary (TDECQ), each lane				3.4	dB
Transmitter eye closure quaternary (TECQ), each lane				3.4	dB
|TECQ-TDECQ|				2.5	dB

Transmitter transition time	17	ps
Transmitter power excursion	1.8	dBm
Transmitter over/undershoot	22	%
Transmitter peak-to-peak power	4.5	dBm
$RIN_{17.1}$ OMA	-136	dB/Hz
Average launch power of OFF transmitter	-16	dBm
Optical return loss tolerance	17.1	dB
Transmitter Reflectance	-26	dB

*15: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

High Speed Optical Receiver Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Optical Characteristics @TP3 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling speed per lane			106.25		Gbps
Center wavelength	λc0	1264.5	1271	1277.5	nm
	λc1	1284.5	1291	1297.5	nm
	λc2	1304.5	1311	1317.5	nm
	λc3	1324.5	1331	1337.5	nm
Damage threshold		5.4			dBm
Average receiver power per lane		-7.2		4.4	dBm
Difference in receive power between any two lane (OMA_{outer})				4.1	dB
Receive outer optical modulation amplitude, each lane	OMA_{outer}			3.7	dBm
Receiver sensitivity (OMA) per Lane	Sen*16			-4.6, TECQ-6.0	dBm
Stressed receiver sensitivity (OMA), each lane	SRS			-2.6	dBm
LOS Assert (Avg.)	LOSA	-15			dBm
LOS De-Assert (Avg.)	LOSD			-10	dBm
RSSI accuracy		-2		+2	dB
Receiver reflectance				-26	dB

*16: Receiver sensitivity, @<4.6dBm, for Tx with TDECQ<1.4dB; @<TECQ-6, for Tx with 3.4dB≥TDECQ≥1.4dB.

*17: Measured with a reference transmitter to produce SECQ greater than or equal to 2dB. The BER at receiver must stay within the specified limit over an OMA range of (-4.9 + TDECQ) dBm to 3.7dBm.

Regulatory Compliance Issues

Various standard and regulations apply to the 800G-OSFP112-2xFR4 modules. These include eye-safety, Component Recognition, RoHS, ESD, EMC and Immunity. Please note the transmitter module is a Class 1 laser product. See Regulatory Compliance Table for details.

Regulatory Compliance Table

Feature	Test Method	Performance
Laser Eye Safety and Equipment Type Testing 	(IEC) EN 62368-1:2014+A11 (IEC) EN 60825-1:2014 (IEC) EN 60825-2:2004+A1+A2	CDRH Accession Number:2132182-000TUV File: R 50457725 0001 CB File: JPTUV-100513
Component Recognition	Underwriters Laboratories (UL) and Canadian Standards Association (CSA) Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File: E317337
RoHS Compliance	RoHS Directive 2011/65/EU&(EU)2015/863	Less than 100 ppm of cadmium. Less than 1000 ppm lead, mercury, hexavalent chromium, poly brominatedbiphenyls (PPB), poly brominated biphenyl ethers (PBDE), dibutyl phthalate, butyl benzyl phthalate, bis (2-ethylhexyl) phthalate and diisobutyl phthalates.
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM)	High speed contacts shall withstand 1000V. All other contacts shall withstand 2000 V.
Electrostatic Discharge (ESD)to the Optical Connector Receptacle	IEC 61000-4-2:2008	When installed in a properly grounded housing and chassis the units are subjected to 15kV air discharges during operation and 8kV direct discharges to the case.
Electromagnetic Interference (EMI)	FCC Part 15 Class B; CISPR 32 (EN55032) 2015;	System margins are dependent on customer board and chassis design.
Immunity	IEC 61000-4-3:2010; EN55035:2017	Typically shows no measurable effect from a 10V/m field swept from 80 MHz to 6 GHz applied to the module without a chassis enclosure.

Electrostatic Discharge (ESD)

The 800G-OSFP112-2xFR4 is compatible with ESD levels found in typical manufacturing and operating environments. As described in the Regulatory Compliance Table. In the normal handling and operation of optical transceivers, ESD is of concern in two circumstances.

The first case is during handling of the transceiver prior to insertion into a OSFP compliant cage. To protect the device, it is important to use normal ESD handling precautions. These include use of grounded wrist straps, workbenches and floor wherever a transceiver is handled.

The second case to consider is static discharges to the exterior of the host equipment chassis after installation. If the optical interface is exposed to the exterior of the host equipment cabinet, the transceiver may be subject to system level ESD requirements.

Electromagnetic Interference (EMI)

Equipment incorporating multi-gigabit transceivers is typically subject to regulation by the FCC in the United States, CENELEC EN55032 (CISPR 32) in Europe. The 800G-OSFP112-2xFR4 compliance to these standards is detailed in the Regulatory Compliance Table. The metal housing and shielded design of the 800G-OSFP112-2xFR4 minimizes the EMI challenge facing the equipment designer.

Flammability

The 800G-OSFP112-2xFR4 optical transceiver is made of metal and high strength, heat resistant, chemicalresistant and UL94V-0 flame retardant plastic.

OSFP Transceiver Electrical Pad Layout

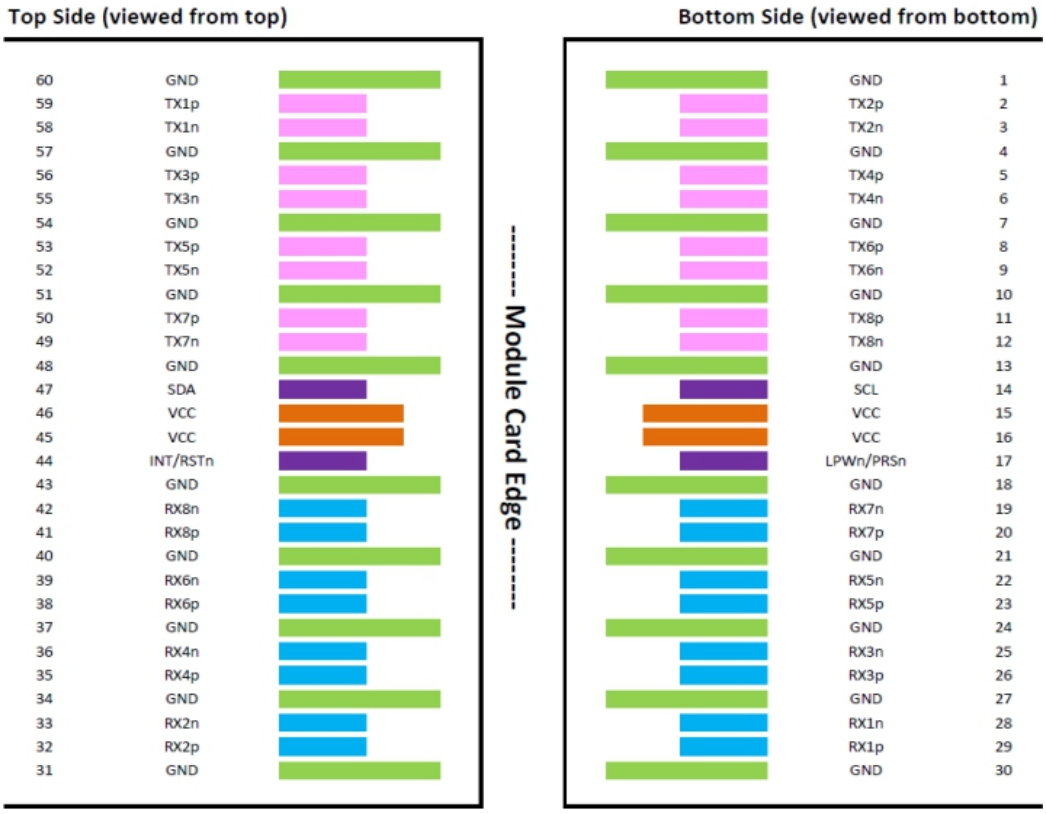

Figure 6: OSFP Module Pinout

Pin Arrangement and Definition

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2p	Transmitter Data Non-Inverted	3	
3	CML-I	Tx2n	Transmitter Data Inverted	3	
4		GND	Ground	1	1
5	CML-I	Tx4p	Transmitter Data Non-Inverted	3	
6	CML-I	Tx4n	Transmitter Data Inverted	3	
7		GND	Ground	1	1
8	CML-I	Tx6p	Transmitter Data Non-Inverted	3	
9	CML-I	Tx6n	Transmitter Data Inverted	3	
10		GND	Ground	1	1
11	CML-I	Tx8p	Transmitter Data Non-Inverted	3	
12	CML-I	Tx8n	Transmitter Data Inverted	3	
13		GND	Ground	1	1
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	3	2
15		VCC	+3.3V Power	2	
16		VCC	+3.3V Power	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present	3	
18		GND	Ground	1	1
19	CML-O	Rx7n	Receiver Data Inverted	3	
20	CML-O	Rx7p	Receiver Data Non-Inverted	3	
21		GND	Ground	1	1
22	CML-O	Rx5n	Receiver Data Inverted	3	
23	CML-O	Rx5p	Receiver Data Non-Inverted	3	
24		GND	Ground	1	1
25	CML-O	Rx3n	Receiver Data Inverted	3	
26	CML-O	Rx3p	Receiver Data Non-Inverted	3	
27		GND	Ground	1	1
28	CML-O	Rx1n	Receiver Data Inverted	3	
29	CML-O	Rx1p	Receiver Data Non-Inverted	3	
30		GND	Ground	1	1
31		GND	Ground	1	1
32	CML-O	Rx2p	Receiver Data Non-Inverted	3	
33	CML-O	Rx2n	Receiver Data Inverted	3	
34		GND	Ground	1	1
35	CML-O	Rx4p	Receiver Data Non-Inverted	3	
36	CML-O	Rx4n	Receiver Data Inverted	3	
37		GND	Ground	1	1
38	CML-O	Rx6p	Receiver Data Non-Inverted	3	
39	CML-O	Rx6n	Receiver Data Inverted	3	
40		GND	Ground	1	1

41	CML-O	Rx8p	Receiver Data Non-Inverted	3	
42	CML-O	Rx8n	Receiver Data Inverted	3	
43		GND	Ground	1	1
44	Multi-Level	INT/RSTn	Module input/Module Reset	3	
45		VCC	+3.3V Power	2	
46		VCC	+3.3V Power	2	
47	LVCMOS-I/O	SCL	2-wire Serial interface Data	3	2
48		GND	Ground	1	1
49	CML-I	Tx7n	Transmitter Data Inverted	3	
50	CML-I	Tx7p	Transmitter Data Non-Inverted	3	
51		GND	Ground	1	1
52	CML-I	Tx5n	Transmitter Data Inverted	3	
53	CML-I	Tx5p	Transmitter Data Non-Inverted	3	
54		GND	Ground	1	1
55	CML-I	Tx3n	Transmitter Data Inverted	3	
56	CML-I	Tx3p	Transmitter Data Non-Inverted	3	
57		GND	Ground	1	1
58	CML-I	Tx1n	Transmitter Data Inverted	3	
59	CML-I	Tx1p	Transmitter Data Non-Inverted	3	
60		GND	Ground	1	1
1: OSFP uses common ground (GND) for all signals and supply (power). All are common within the OSFP module and all module voltages are referenced to this potential unless otherwise noted.					
2: Open-Drain with pull up resistor on Host.					

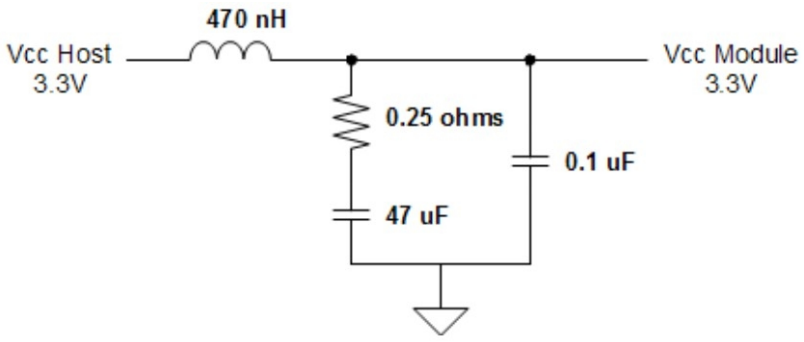

Figure 7: Recommended Host Board Power Supply Filter

For safety and protection of the host system, the power to each OSFP module may be protected by an electronic circuit breaker on the host board which is enabled with the H_PRSn signal such that power is only enabled when the module is fully engaged into the OSFP connector.

Package Outline

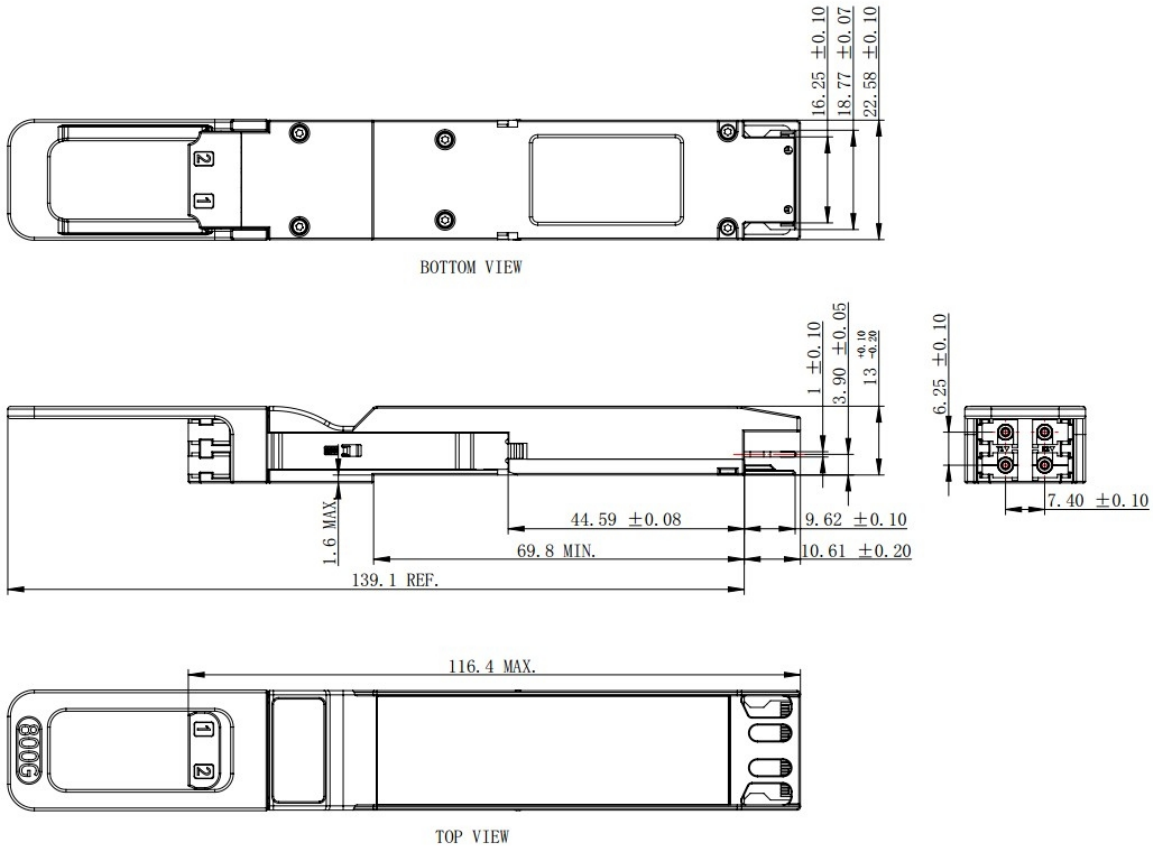

Figure 8: Mechanical Package Outline (All dimensions in mm)

*This 2D drawing is only for reference, please check with Do-Networks before ordering.

The bellow picture shows the location of the hottest spot for measuring module case temperature. In addition, the digital diagnostic monitors (DDM) temperature is also calibrated to this spot.

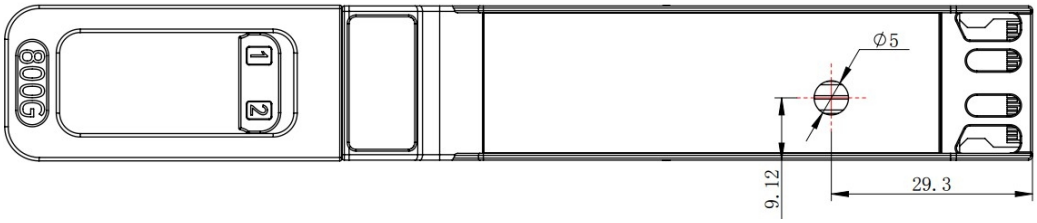

Figure 9: Case Temperature Measurement Point (All dimensions in mm)

The optical interface port is a Dual Duplex LC connector.

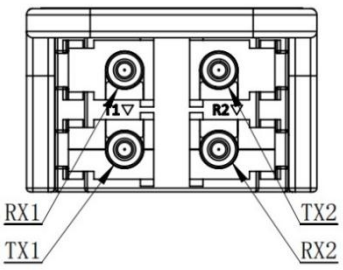

Figure 10: Module Optical Interface (looking into the optical port)

Control Interface & Memory Map

The control interface combines dedicated signal lines for LPWn/PRSn, INT/RSTn with two-wire serial (TWS), interface clock (SCL) and data (SDA), signals to provide users rich functionality over an efficient and easily used interface.

SCL and SDA

SCL and SDA are a 2-wire serial interface between the host and module using the I2C protocols. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3Von the host. The pull-up resistor value shall be 1k ohms to 4.7k ohms depending on capacitive load.

This 2-wire interface supports bus speeds:

- Required - I2C Fast-mode (Fm) ≤ 400 kbit/s
- Optional - I2C Fast-mode Plus (Fm+) ≤ 1 Mbit/s

The host shall default to using 100 kbit/s standard-mode I2C when first accessing an unidentified module for backward compatibility. Once the module has been brought out of reset, the host can read the module's 2-wire interface speed register to determine the maximum supported speed the module allows. For an OSFP, the host may then use I2C Fast-mode, I2C Fast-mode Plus Single Data Rate, as indicated by the module. It is optional for the host to change the speed of the 2-wire interface but remaining at a low speed could lead to slow management transactions for modules that require frequent accesses.

SCL and SDA signals follow the electrical specifications of Fast-mode, and Fast-mode Plus as defined in the I2C -bus specification.

SCL and SDA Pin Electrical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit
SCL and SDA	VOL	0		0.4	V
	VOH	VCC-0.5		VCC+0.3	V
SCL and SDA	VIL	-0.3		VCC*0.3	V
	VIH	VCC*0.7		VCC+0.5	V

INT/RSTn

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. The circuit shown in OSFP MSA Figure11-3 enables multi-level signaling to provide direct signal control in both directions. Reset is an active low signal on the host which is translated to an active-low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active-low signal on the host.

The INT/RSTn signal operates in 3 voltage zones to indicate the state of Reset for the module and Interrupt for the host. Figure 11 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_INTn signal and the module uses a voltage reference at 1.25V to determine the state of the M_RSTn signal.

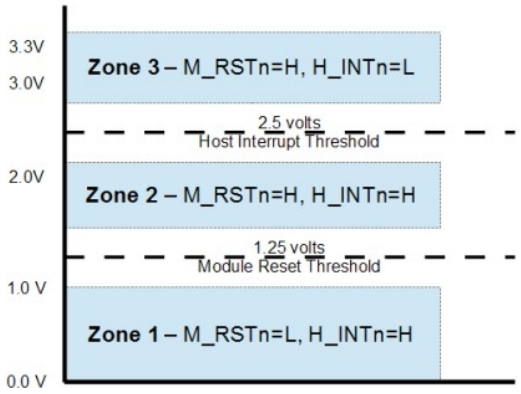

Figure 11: INT/RSTn Voltage Zones

LPWn/PRSn

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. The circuit shown in OSFP MSA Figure11-5 enables multi-level signaling to provide direct signal control in both directions. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.

The LPWn/PRSn signal operates in 3 voltage zones to indicate the state of Low Power mode for the module and Module Present for the host. Figure 12 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_PRSn signal and the module uses a voltage reference at 1.25V to determine the state of the M_LPWn signal.

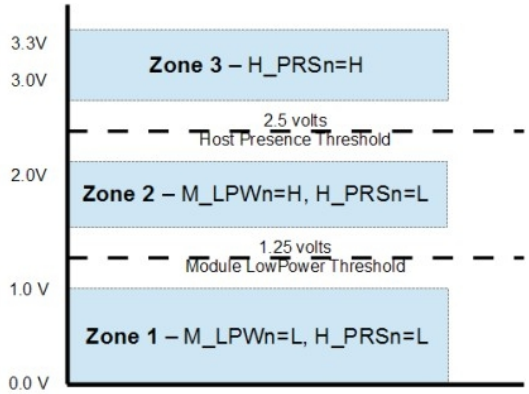

Figure 12: LPWn/PRSn Voltage Zones

Timing for control and status functions

Parameter	Symbol	Min.	Typical	Max.	Unit
MgmtInit duration	t_init			2000	ms
ResetL assert time	t_reset_init	10			μs
Reset assert time	t_reset			8	s
LPMode assert time	ton_LPMode			200	μs
LPMode de-assert time	toff_LPMode			8	s
IntL assert time	ton_IntL			200	ms
IntL de-assert time	toff_IntL			500	μs

Rx LOS assert time	ton_LOS	100	ms
Tx fault assert time	ton_flag	200	ms
Flag assert time	ton_flag	200	ms
Mask assert time	ton_mask	100	ms
Mask de-assert time	toff_mask	100	ms
Application or rate select change time	t_ratesel	8	s
Rx squelch assert time	ton_Rxsq	15	ms
Rx squelch de-assert time	toff_Rxsq	5000	ms
Tx squelch assert time	ton_Txsq	400	ms
Tx squelch de-assert time	toff_Txsq	5000	ms
Tx disable assert time	ton_txdis	100	ms
Tx disable de-asssert time	toff_txdis	400	ms
Rx output disable assert time	ton_rxdis	100	ms
Rx output disable de-assert time	toff_rxdis	100	ms
Squelch disable assert time	ton_sqdis	100	ms
Squelch disable de-assert time	toff_sqdis	100	ms

Memory Map

The control interface and memory map of the OSFP module is compliant with the CMIS. The OSFP module support I2C interface protocol defined by the CMIS. Access clock frequency support a minimum of 100 kHz with no clock stretching.

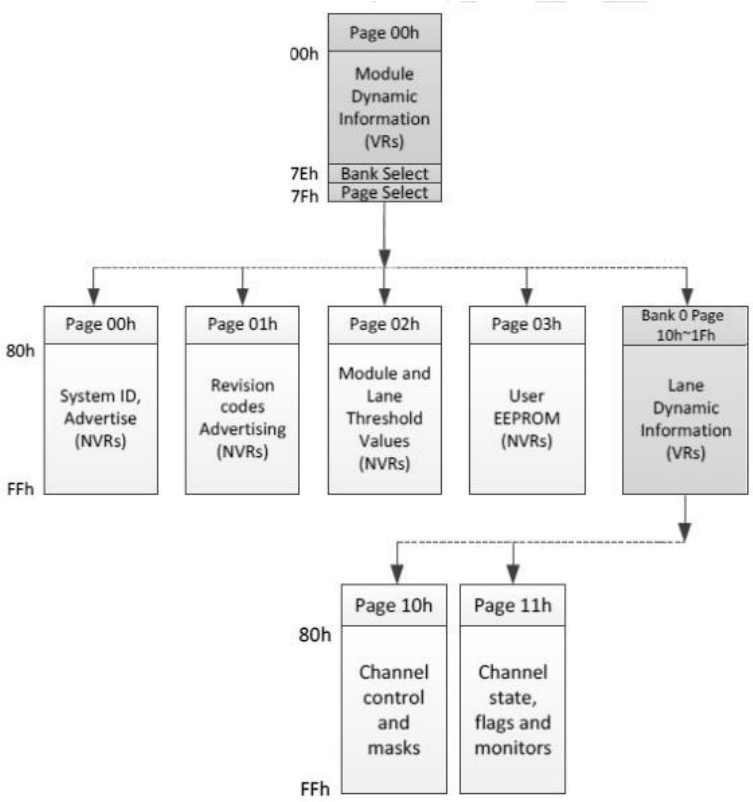

Figure 13: Simplified CMIS Module Memory Map Architecture

Revision History

Revision	Initiated	Reviewed	Approved	Revision History	Release Date
V1.a	Kurt	Dony/Julian/ Lanne/Angela		Preliminary.	Jan 26, 2024

Quality

Do-Networks Technology has passed many quality system verifications, established an internationally standardized quality assurance system and strictly implemented standardized management and control in the course of design, development, production, installation and service. For latest certification/accreditation numbers, please, contact us.

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