

## Product Description

Do-Networks's OSFP transceiver module is designed for use in 800 Gigabit Ethernet links over 10km single mode fiber. The module has 8 independent electrical input/output channels operating up to 106.25Gbps per channel. This transceiver consists of two transmitter/receiver units, with each operating on a set of 4 wavelengths on the ITU G.694.2 CWDM grid near 1300nm. The transmitter path of the module incorporates a bi-directional PAM4 re-timer ASIC integrated with an 8-channels modulator driver, 8 externally modulated lasers and two optical multiplexers. On the receiver path, two optical de-multiplexers are coupled to 8 photodiodes and two 4-channel TIA arrays, along with the PAM4 re-timer. The electrical interface of the module is compliant with the 800GAUI-8 interface as defined by IEEE 802.3ck, and compliant with OSFP MSA.

## Features

- Supports 850Gbps
- Single 3.3V Power Supply
- Up to 10km over SMF with KP4 FEC supported at the Host side
- Dual duplex LC connector
- 8x106.25Gbps (PAM4) electrical interface
- PIN and TIA array on the receiver side
- Power dissipation < 17W
- Case temperature range: 0°C to 70°C (commercial)
- Safety Certification: TUV/UL/FDA\*<sup>1</sup>
- RoHS Compliant

## Applications\*<sup>1</sup>

- 1x800G Ethernet
- 2x400G Ethernet
- 2x200G Ethernet

## Ordering Information

| Part No.           | Data Rate | Fiber | Distance* <sup>2</sup> | Interface      | Temp.  | DDMI | CMIS                  |
|--------------------|-----------|-------|------------------------|----------------|--------|------|-----------------------|
| 800G-OSFP112-2xLR4 | 850Gbps   | SMF   | 10km                   | Dual duplex LC | 0~70°C | Yes  | CMIS5.0* <sup>3</sup> |

\*1: For more details, please contact with Do-Networks.

\*2: Over G.652 SMF.

\*3: CMIS5.0 or later version.

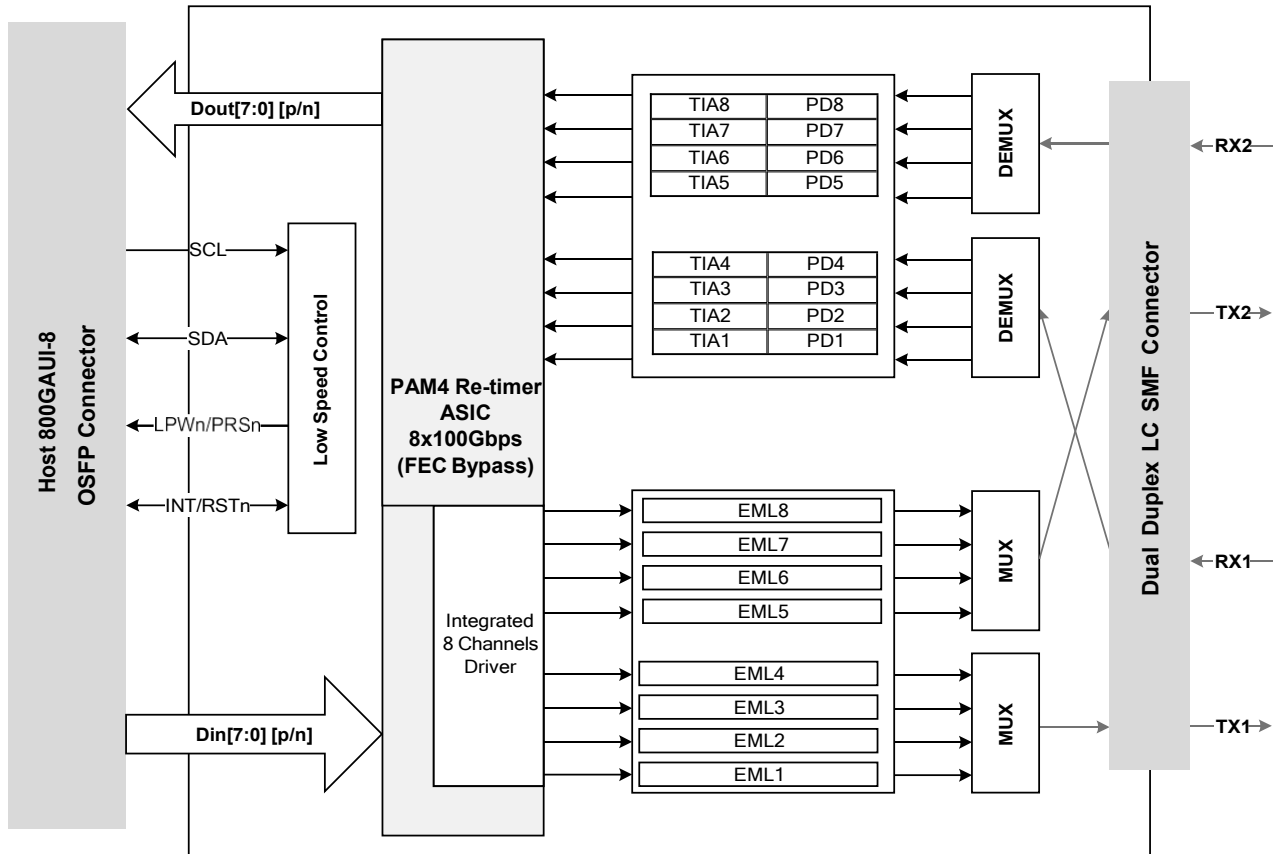


Figure 1: Transceiver Block Diagram

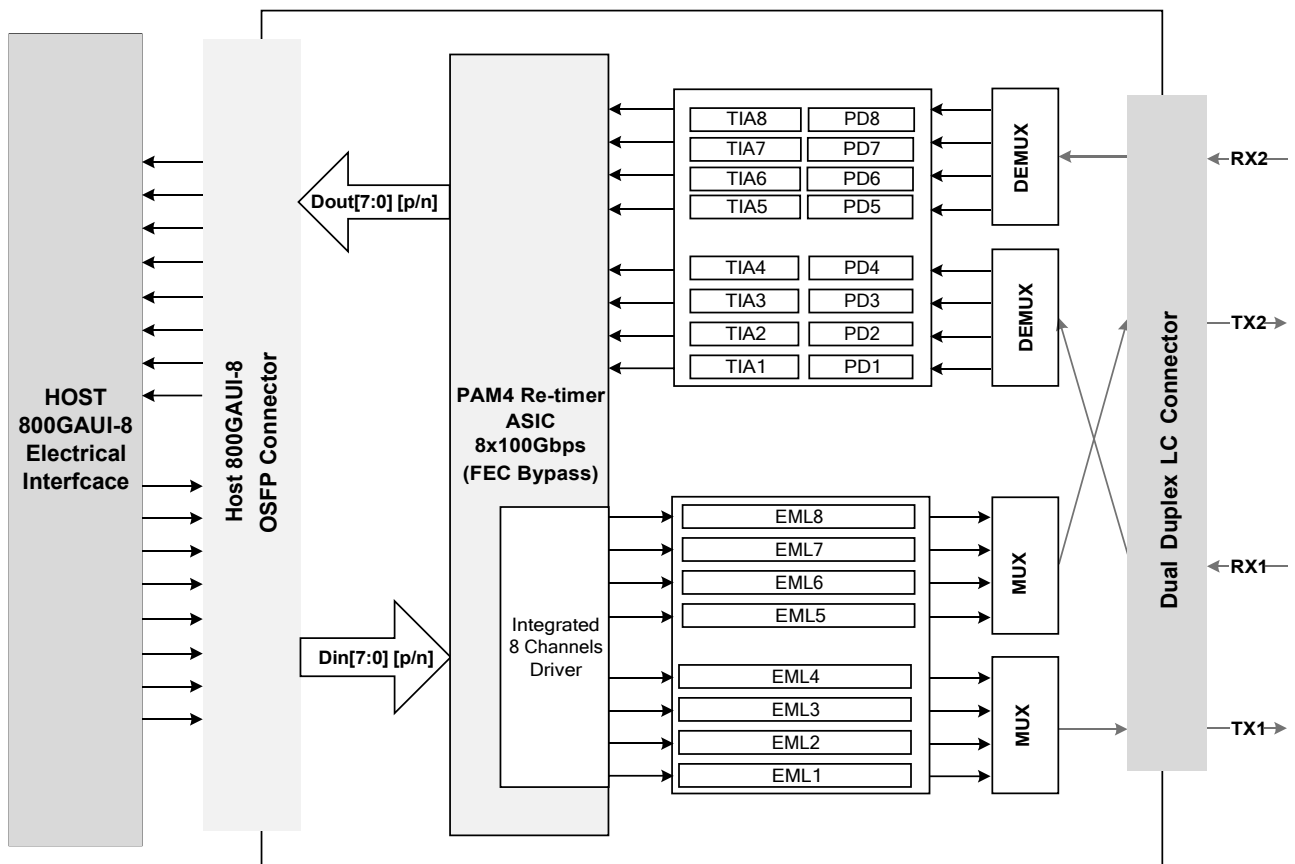


Figure 2: Application Reference Diagram

## Transmitter

As shown in Figure 1, the transmitter path of the transceiver contains an 8x100Gbps 800GAUI-8 electrical input with Equalization (EQ) block, integrated electrical multiplexer, integrated 8 Channels driver, 8 externally modulated lasers, optical multiplexer and diagnostic monitors. The integrated electrical multiplexer and integrated driver converts 8 channels of 100Gbps (PAM4) electrical input data to 8 channels of 100Gbps (PAM4) parallel optical signals. The transmitter complies with EN 60825 and CDRH Class 1 human eye safety compliance.

## Receiver

As shown in Figure 1, the receiver path of the transceiver contains optical de-multiplexer, eight PIN photodiodes, trans-impedance amplifiers (TIA), integrated de-multiplexer and 8x100G 800GAUI-8 compliant electrical output blocks. The PIN-TIA and integrated de-multiplexer converts 8 channels of 100Gbps (PAM4) parallel optical signals to 8 channels of 100Gbps (PAM4) electrical output data.

## High Speed Electrical Signal Interface

The interface between OSFP module and ASIC/SerDes is shown in Figure 2. The high speed signal lines are internally AC-coupled and the electrical inputs are internally terminated to 100 Ohms differential. All transmitter and receiver electrical channels are compliant to module 800GAUI-8 specifications per IEEE 802.3ck.

## Control Signal Interface

The control signal interface is compliant with OSF MSA. The following pin is provided to control module or display the module status: LPWn/PRSn, INT/RSTn. In addition, there is an industry standard two wire serial interface scaled for 3.3V LVTTL. The definition of control signal interface and the registers of the serial interface memory are defined in the Control Interface & Memory Map section.

## Handling and Cleaning

Exposure to current surges and overvoltage events can cause immediate damage to the transceiver module. Observe the precautions for normal operation of electrostatic discharge sensitive equipment; Attention shall also be paid to limiting transceiver module exposure to conditions beyond those specified in the absolute maximum ratings.

Optical connectors include female connectors. These elements will be exposed as long as the cable or port plug is not inserted. At this time, always pay attention to protection.

Each module is equipped with a port guard plug to protect the optical port. The protective plug shall always be in place whenever the optical fiber is not inserted. Before inserting the optical fiber, it is recommended to clean the end of the optical fiber connector to avoid contamination of the module optical port due to dirty connector. If contamination occurs, use standard LC port cleaning methods.

## Absolute Maximum Ratings\*<sup>4</sup>

Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operating Conditions. It should not be assumed that limiting values of more than one parameter can be applied to the module concurrently. Exposure to any of the Absolute Maximum Ratings for extended periods can adversely affect reliability.

| Parameter                                       | Symbol          | Min. | Typical | Max.                 | Unit |
|-------------------------------------------------|-----------------|------|---------|----------------------|------|
| Storage Temperature                             | T <sub>s</sub>  | -40  |         | 85                   | °C   |
| 3.3 V Power Supply Voltage                      | V <sub>cc</sub> | -0.5 | 3.3     | 3.6                  | V    |
| Data Input Voltage - Single Ended               |                 | -0.5 |         | V <sub>cc</sub> +0.5 | V    |
| Data Input Voltage - Differential* <sup>5</sup> |                 |      |         | 0.8                  | V    |
| Relative Humidity                               | RH              | 5    |         | 95                   | %    |

\*4: Exceeding any one of these values may damage the device permanently.

\*5: This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry. The damage threshold of the module input shall be at least 1600 mV peak to peak differential.

## Recommended Operating Conditions\*<sup>6</sup>

For operations beyond the recommended operating conditions, optical and electrical characteristics are not defined, reliability is not implied, and such operations for a long time may damage the module.

| Parameter                                                      | Symbol          | Min.  | Typical | Max.  | Unit |
|----------------------------------------------------------------|-----------------|-------|---------|-------|------|
| Operating case temperature* <sup>7</sup>                       | T <sub>c</sub>  | 0     |         | 70    | °C   |
| Storage temperature                                            | T <sub>s</sub>  | -40   |         | +85   | °C   |
| Power supply voltage                                           | V <sub>cc</sub> | 3.135 | 3.3     | 3.465 | V    |
| Power dissipation                                              | P <sub>D</sub>  |       |         | 17    | W    |
| Electrical Signal Rate per Channel (PAM encoded)* <sup>8</sup> |                 |       | 53.125  |       | GBb  |
| Optical Signal Rate per Channel (PAM encoded)* <sup>9</sup>    |                 |       | 53.125  |       | GBd  |
| Power Supply Noise* <sup>10</sup>                              |                 |       |         | 66    | mVpp |
| Receiver Differential Data Output Load                         |                 | 100   |         |       | Ohm  |
| Fiber Length (9um SMF)* <sup>11</sup>                          |                 |       |         | 10    | km   |

\*6: Power Supply specifications, Instantaneous, sustained and steady state current compliant with OSFP MSA Power Classification.

\*7: The position of case temperature measurement is shown in Figure 9.

\*8: 800GAUI-8 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.

\*9: 800G 2×LR4 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.

\*10: Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 7 for recommended power supply filter.

\*11: 9µm SMF. The maximum link distance is based on an allocation of 3dB of attenuation and 3dB total connection and splice loss. The loss of a single connection shall not exceed 0.5dB.

## General Electrical Characteristics\*12

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

| Parameter                               | Symbol | Min. | Typical | Max. | Unit |
|-----------------------------------------|--------|------|---------|------|------|
| Transceiver Power Consumption           |        |      | 14.5    | 17   | W    |
| Transceiver Power Supply Current, Total |        |      |         | 5420 | mA   |
| AC coupling capacitors (Internal)       |        |      | 0.1     |      | uF   |

\*12: For control signal timing including LPWn/PRSn, INT/RSTn, SCL and SDA see Control Interface Section

## Reference Points

| Test Point               | Description                                                                                                                                                                                                                                                                |
|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TP0 to TP5               | The channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.                                                                                                           |
| TP1 to TP4               | All cable assembly measurements are made between TP1 and TP4 as illustrated in Figure 3.                                                                                                                                                                                   |
| TP0 to TP2<br>TP3 to TP5 | A mated connector pair has been included in both the transmitter and receiver specifications defined in 802.3ck 162.9.3 and 162.9.4. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided in 802.3ck 162.9.3.2 |
| TP2                      | Unless specified otherwise, all transmitter measurements defined in 802.3ck 162.9.3 are made at TP2 utilizing the test fixture specified in Annex 162B.                                                                                                                    |
| TP3                      | Unless specified otherwise, all receiver measurements and tests defined in 802.3ck 162.9.4 are made at TP3 utilizing the test fixture specified in Annex 162B.                                                                                                             |

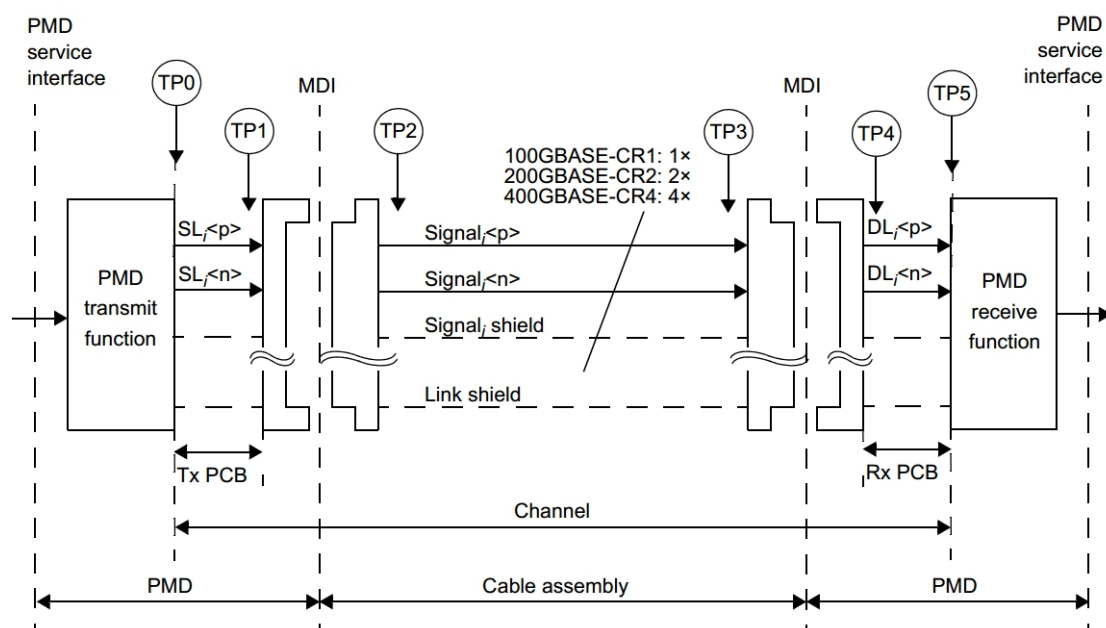


Figure 3: IEEE 802.3ck 100GBASE-CR1, 200GBASE-CR2 or 400GBASE-CR4 link

The diagram illustrates the interface between the MCB and the Module. The MCB is represented by a large rectangle on the left. The Module is represented by a dashed-line boundary on the right. Inside the Module, there is a Receiver and a Transmitter. The Receiver is labeled "100GAUI-1, 200GAUI-2, or 400GAUI-4 module component". The Transmitter is labeled "Transmitter". TP1 (Transmit Port 1) is connected to the Receiver, and TP4 (Transmit Port 4) is connected to the Transmitter. The Receiver and Transmitter are connected to the MCB via a vertical interface line.

| Parameter                                         | Test Point | Min.                 | Typical           | Max. | Unit | Conditions  |
|---------------------------------------------------|------------|----------------------|-------------------|------|------|-------------|
| Signaling Rate, Per Lane<br>(PAM4 encoded)        | TP1        |                      | 53.125            |      | GBd  | +/- 100 ppm |
| Differential peak-peak Input<br>Voltage Tolerance | TP1a       | 750                  |                   |      | mV   |             |
| AC common-mode RMS<br>voltage tolerance           | TP1a       | 25                   |                   |      | mV   |             |
| Differential-mode to<br>common-mode return loss   | TP1        | Equation<br>(120G-2) |                   |      | dB   | 802.3ck     |
| Effective return loss, ERL                        | TP1        | 8.5                  |                   |      | dB   |             |
| Differential termination<br>mismatch              | TP1        |                      |                   | 10   | %    |             |
| Module stressed input<br>tolerance                | TP1a       |                      | See<br>120G.3.4.3 |      |      | 802.3ck     |
| Single-ended voltage<br>tolerance range           | TP1a       | -0.4                 |                   | 3.3  | V    |             |
| DC common-mode voltage<br>tolerance range         | TP1        | -350                 |                   | 2850 | mV   |             |
| Module stressed input tolerance test :            |            |                      |                   |      |      |             |

|                                             |              |      |         |
|---------------------------------------------|--------------|------|---------|
| Pattern generator transition time           | 9            |      | ps      |
| Applied peak-peak sinusoidal jitter         | Table 162-16 |      | 802.3ck |
| Eye height                                  | 10           |      | mV      |
| Vertical eye closure, VEC                   | 12           | 12.5 | dB      |
| Crosstalk differential peak-to-peak voltage | 845          |      | mV      |
| Crosstalk transition time                   | 8.5          |      | ps      |

## High Speed Electrical Output Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

| Parameter                                                          | Test Point | Min.              | Typical                            | Max.       | Unit |
|--------------------------------------------------------------------|------------|-------------------|------------------------------------|------------|------|
| Signaling Rate, Per Lane (range)                                   | TP4        |                   | 53.125 <sup>*13</sup><br>± 100 ppm |            | GBd  |
| AC common-mode output voltage                                      | TP4        |                   |                                    | 25         | mV   |
| Differential peak-to-peak input voltage<br>Short mode<br>Long mode | TP4        |                   |                                    | 600<br>845 | mV   |
| Eye height                                                         | TP4        | 15                |                                    |            | mV   |
| Vertical eye closure                                               | TP4        |                   |                                    | 12         | dB   |
| Effective return loss                                              | TP4        | 8.5               |                                    |            | dB   |
| Common-mode to differential-mode return loss                       | TP4        | Equation (120G-1) |                                    |            | dB   |
| Differential termination mismatch                                  | TP4        |                   |                                    | 10         | %    |
| Transition time                                                    | TP4        | 8.5               |                                    |            | ps   |
| DC common-mode voltage tolerance                                   | TP4        | -0.35             |                                    | 2.85       | V    |

\*13: The signaling rate range is derived from the PMD receiver input.

## High Speed Optical Transmitter Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

### Optical Characteristics @TP2 Test Point

| Parameter                  | Symbol         | Min.   | Typical         | Max.   | Unit |
|----------------------------|----------------|--------|-----------------|--------|------|
| Signaling speed per lane   |                |        | 53.125 ± 100ppm |        | GBd  |
| Modulation format          |                |        | PAM4            |        |      |
| Lane_1/5 Center Wavelength | $\lambda_{C0}$ | 1264.5 | 1271            | 1277.5 | nm   |
| Lane_2/6 Center Wavelength | $\lambda_{C1}$ | 1284.5 | 1291            | 1297.5 | nm   |

|                                                                                                                                        |                |                  |      |        |       |
|----------------------------------------------------------------------------------------------------------------------------------------|----------------|------------------|------|--------|-------|
| Lane_3/7 Center Wavelength                                                                                                             | $\lambda_{C2}$ | 1304.5           | 1311 | 1317.5 | nm    |
| Lane_4/8 Center Wavelength                                                                                                             | $\lambda_{C3}$ | 1324.5           | 1331 | 1337.5 | nm    |
| Side-mode Suppression Ratio                                                                                                            | SMSR           | 30               |      |        | dB    |
| Total average launch power                                                                                                             |                |                  |      | 11.1   | dBm   |
| Average launch power, each lane <sup>*14</sup>                                                                                         | TxAVG          | -2.7             |      | 5.1    | dBm   |
| Outer Optical Modulation Amplitude (OMA <sub>outer</sub> ), each lane <sup>*15</sup><br>for TDECQ < 1.4dB<br>for 1.4dB ≤ TDECQ ≤ 3.9dB | TxOMA          | 0.3<br>TDECQ-1.1 |      | 4.4    | dBm   |
| Difference in launch power between any two lanes (OMA <sub>outer</sub> )                                                               |                |                  |      | 4      | dB    |
| Transmitter and dispersion eye closure for PAM4 (TDECQ) , each lane                                                                    | TDECQ          |                  |      | 3.9    | dB    |
| Transmitter eye closure for PAM4 (TECQ) , each lane                                                                                    | TECQ           |                  |      | 3.9    | dB    |
| TDECQ-TECQ                                                                                                                             |                |                  |      | 2.5    | dB    |
| Average launch power of OFF transmitter, each lane                                                                                     |                |                  |      | -16    | dBm   |
| Extinction Ratio                                                                                                                       | ER             | 3.5              |      |        | dB    |
| Transmitter transition time                                                                                                            |                |                  |      | 17     | ps    |
| Over/under-shoot                                                                                                                       |                |                  |      | 25     | %     |
| Transmitter peak-to-peak power                                                                                                         |                |                  |      | 5.2    | dBm   |
| RIN <sub>15.6</sub> OMA                                                                                                                |                |                  |      | -136   | dB/Hz |
| Optical return loss tolerance                                                                                                          |                |                  |      | 15.6   | dB    |
| Transmitter reflectance <sup>*16</sup>                                                                                                 |                |                  |      | -26    | dB    |

\*14: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

\*15: Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 4.5 dB or TDECQ < 1.3 dB for an extinction ratio of < 4.5 dB, the OMA<sub>outer</sub> (min) must exceed this value.

\*16: Transmitter reflectance is defined looking into the transmitter.

## High Speed Optical Receiver Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

### Optical Characteristics @TP3 Test Point

| Parameter                  | Symbol         | Min.   | Typical         | Max.   | Unit |
|----------------------------|----------------|--------|-----------------|--------|------|
| Signaling speed per lane   |                |        | 53.125 ± 100ppm |        | GBd  |
| Modulation format          |                |        | PAM4            |        |      |
| Lane_1/5 Center Wavelength | $\lambda_{C0}$ | 1264.5 | 1271            | 1277.5 | nm   |
| Lane_2/6 Center Wavelength | $\lambda_{C1}$ | 1284.5 | 1291            | 1297.5 | nm   |
| Lane_3/7 Center Wavelength | $\lambda_{C2}$ | 1304.5 | 1311            | 1317.5 | nm   |
| Lane_4/8 Center Wavelength | $\lambda_{C3}$ | 1324.5 | 1331            | 1337.5 | nm   |

|                                                                                                                         |        |      |                  |     |
|-------------------------------------------------------------------------------------------------------------------------|--------|------|------------------|-----|
| Damage threshold each lane <sup>*17</sup>                                                                               |        | 6.1  |                  | dBm |
| Average receive power each lane <sup>*18</sup>                                                                          | RxAVG  | -9   | 5.1              | dBm |
| Receive Power (OMA <sub>outer</sub> ) each lane                                                                         | RxOMA  |      | 4.4              | dBm |
| Difference in receive power between any two lanes (OMA <sub>outer</sub> )                                               |        |      | 4.3              | dB  |
| Receiver reflectance                                                                                                    |        |      | -26              | dB  |
| Receiver sensitivity (OMA <sub>outer</sub> ), each lane <sup>*19</sup><br>for TDECQ < 1.4dB<br>for 1.4dB < TECQ < 3.4dB | SenOMA |      | -6.8<br>TECQ-8.2 | dBm |
| Stressed receiver sensitivity (OMA <sub>outer</sub> ), each lane                                                        |        |      | -4.3             |     |
| Conditions of stressed receiver sensitivity test <sup>*20</sup> :                                                       |        |      |                  |     |
| Stressed eye closure for PAM4 (SECQ), lane under test                                                                   |        |      | 3.9              | dB  |
| OMA <sub>outer</sub> of each aggressor lane                                                                             |        | -0.4 |                  | dBm |
| LOS Assert                                                                                                              | LOSA   | -15  |                  | dBm |
| LOS De-Assert                                                                                                           | LOSD   |      | -10              | dBm |
| LOS Hysteresis                                                                                                          |        | 0.5  |                  | dB  |

\*17: The receiver shall be able to tolerate, without damage, continuous exposure to an optical signal having this average power level. The receiver does not have to operate correctly at this input power.

\*18: Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

\*19: Measured with conformance test signal at TP3 for the BER specified in IEEE Std 802.3-2018 clause.

\*20: These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver

## Electrical to Optical Channel Mapping

| Electrical Channels | Optical Wavelength (nm) |
|---------------------|-------------------------|
| 1                   | 1271                    |
| 2                   | 1291                    |
| 3                   | 1311                    |
| 4                   | 1331                    |
| 5                   | 1271                    |
| 6                   | 1291                    |
| 7                   | 1311                    |
| 8                   | 1331                    |

## Regulatory Compliance Issues

Various standard and regulations apply to the 800G-OSFP112-2xLR4 modules. These include eye-safety, Component Recognition, RoHS, ESD, EMC and Immunity. Please note the transmitter module is a Class 1 laser product. See Regulatory Compliance Table for details.

### Regulatory Compliance Table

| Feature                                                                                                                          | Test Method                                                                                                                                                                      | Performance                                                                                                                                                                                                                                                      |
|----------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Laser Eye Safety and Equipment Type Testing<br> | (IEC) EN 62368-1:2014+A11<br>(IEC) EN 60825-1:2014<br>(IEC) EN 60825-2:2004+A1+A2                                                                                                | CDRH Accession Number:2132182-000<br>TUV File: R 50457725 0001<br>CB File: JPTUV-100513                                                                                                                                                                          |
| Component Recognition                                                                                                            | Underwriters Laboratories (UL) and Canadian Standards Association (CSA) Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment | UL File: E317337                                                                                                                                                                                                                                                 |
| RoHS Compliance                                                                                                                  | RoHS Directive 2011/65/EU & (EU)2015/863                                                                                                                                         | Less than 100 ppm of cadmium. Less than 1000 ppm lead, mercury, hexavalent chromium, poly brominated biphenyls (PBB), poly brominated biphenyl ethers (PBDE), dibutyl phthalate, butyl benzyl phthalate, bis (2-ethylhexyl) phthalate and diisobutyl phthalates. |
| Electrostatic Discharge (ESD) to the Electrical Contacts                                                                         | JEDEC Human Body Model (HBM)                                                                                                                                                     | High speed contacts shall withstand 1000V. All other contacts shall withstand 2000 V.                                                                                                                                                                            |
| Electrostatic Discharge (ESD) to the Optical Connector Receptacle                                                                | IEC 61000-4-2:2008                                                                                                                                                               | When installed in a properly grounded housing and chassis the units are subjected to 15kV air discharges during operation and 8kV direct discharges to the case.                                                                                                 |
| Electromagnetic Interference (EMI)                                                                                               | FCC Part 15 Class B; CISPR 32 (EN55032) 2015;                                                                                                                                    | System margins are dependent on customer board and chassis design.                                                                                                                                                                                               |
| Immunity                                                                                                                         | IEC 61000-4-3:2010; EN55035:2017                                                                                                                                                 | Typically shows no measurable effect from a 10V/m field swept from 80 MHz to 6 GHz applied to the module without a chassis enclosure.                                                                                                                            |

## Electrostatic Discharge (ESD)

The 800G-OSFP112-2xLR4 is complying with the ESD requirements described in the Regulatory Compliance Table. However, in the normal processing and operation of optical transceiver, the following two types of situations need special attention.

Case I: Before inserting the transceiver into the rack meeting the requirements of OSFP compliant cage, ESD preventive measures must be taken to protect the equipment. For example, the grounding wrist strap, workbench and floor should be used wherever the transceiver is handled.

Case II: After the transceiver is installed, the electrostatic discharge outside the chassis of the host equipment shall be within the scope of system level ESD requirements. If the optical interface of the transceiver is exposed outside the host equipment cabinet, the transceiver may be subject to equipment system level ESD requirements.

## Electromagnetic Interference (EMI)

Communication equipment with optical transceivers is usually regulated by FCC in the United States and CENELEC EN55032 (CISPR 32) in Europe. The compliance of 800G-OSFP112-2xLR4 with these standards is detailed in the regulatory compliance table. The metal shell and shielding design of 800G-OSFP112-2xLR4 will help equipment designers minimize the equipment level EMI challenges they face.

## Flammability

800G-OSFP112-2xLR4 optical transceiver meets UL certification requirements, its constituent materials have heat and corrosion resistance, and the plastic parts meet UL94V-0 requirements.

## OSFP Transceiver Electrical Pad Layout

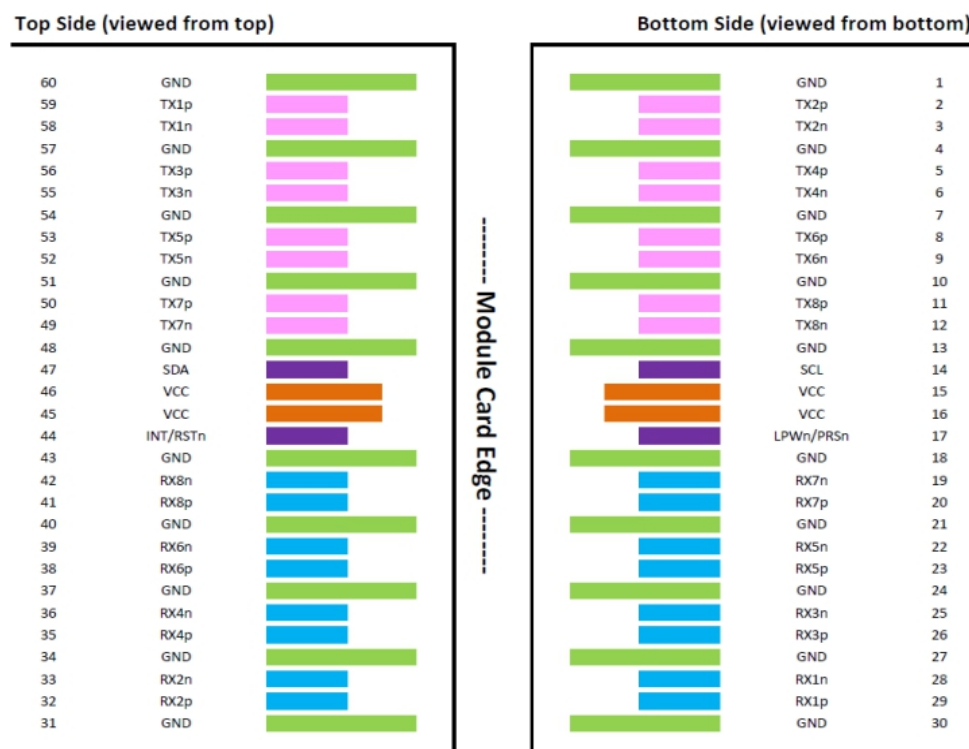


Figure 6: OSFP Module Pinout

## Pin Arrangement and Definition

| Pin | Logic           | Symbol    | Description                   | Plug Sequence | Notes |
|-----|-----------------|-----------|-------------------------------|---------------|-------|
| 1   |                 | GND       | Ground                        | 1             | 1     |
| 2   | CML-I           | Tx2p      | Transmitter Data Non-Inverted | 3             |       |
| 3   | CML-I           | Tx2n      | Transmitter Data Inverted     | 3             |       |
| 4   |                 | GND       | Ground                        | 1             | 1     |
| 5   | CML-I           | Tx4p      | Transmitter Data Non-Inverted | 3             |       |
| 6   | CML-I           | Tx4n      | Transmitter Data Inverted     | 3             |       |
| 7   |                 | GND       | Ground                        | 1             | 1     |
| 8   | CML-I           | Tx6p      | Transmitter Data Non-Inverted | 3             |       |
| 9   | CML-I           | Tx6n      | Transmitter Data Inverted     | 3             |       |
| 10  |                 | GND       | Ground                        | 1             | 1     |
| 11  | CML-I           | Tx8p      | Transmitter Data Non-Inverted | 3             |       |
| 12  | CML-I           | Tx8n      | Transmitter Data Inverted     | 3             |       |
| 13  |                 | GND       | Ground                        | 1             | 1     |
| 14  | LVCMO<br>S-I/O  | SCL       | 2-wire Serial interface clock | 3             | 2     |
| 15  |                 | VCC       | +3.3V Power                   | 2             |       |
| 16  |                 | VCC       | +3.3V Power                   | 2             |       |
| 17  | Multi-Le<br>vel | LPWn/PRSn | Low-Power Mode/Module Present | 3             |       |
| 18  |                 | GND       | Ground                        | 1             | 1     |
| 19  | CML-O           | Rx7n      | Receiver Data Inverted        | 3             |       |
| 20  | CML-O           | Rx7p      | Receiver Data Non-Inverted    | 3             |       |
| 21  |                 | GND       | Ground                        | 1             | 1     |
| 22  | CML-O           | Rx5n      | Receiver Data Inverted        | 3             |       |
| 23  | CML-O           | Rx5p      | Receiver Data Non-Inverted    | 3             |       |
| 24  |                 | GND       | Ground                        | 1             | 1     |
| 25  | CML-O           | Rx3n      | Receiver Data Inverted        | 3             |       |
| 26  | CML-O           | Rx3p      | Receiver Data Non-Inverted    | 3             |       |
| 27  |                 | GND       | Ground                        | 1             | 1     |
| 28  | CML-O           | Rx1n      | Receiver Data Inverted        | 3             |       |
| 29  | CML-O           | Rx1p      | Receiver Data Non-Inverted    | 3             |       |
| 30  |                 | GND       | Ground                        | 1             | 1     |
| 31  |                 | GND       | Ground                        | 1             | 1     |
| 32  | CML-O           | Rx2p      | Receiver Data Non-Inverted    | 3             |       |
| 33  | CML-O           | Rx2n      | Receiver Data Inverted        | 3             |       |
| 34  |                 | GND       | Ground                        | 1             | 1     |
| 35  | CML-O           | Rx4p      | Receiver Data Non-Inverted    | 3             |       |
| 36  | CML-O           | Rx4n      | Receiver Data Inverted        | 3             |       |
| 37  |                 | GND       | Ground                        | 1             | 1     |
| 38  | CML-O           | Rx6p      | Receiver Data Non-Inverted    | 3             |       |
| 39  | CML-O           | Rx6n      | Receiver Data Inverted        | 3             |       |

|    |             |          |                               |   |   |
|----|-------------|----------|-------------------------------|---|---|
| 40 |             | GND      | Ground                        | 1 | 1 |
| 41 | CML-O       | Rx8p     | Receiver Data Non-Inverted    | 3 |   |
| 42 | CML-O       | Rx8n     | Receiver Data Inverted        | 3 |   |
| 43 |             | GND      | Ground                        | 1 | 1 |
| 44 | Multi-Level | INT/RSTn | Module input/Module Reset     | 3 |   |
| 45 |             | VCC      | +3.3V Power                   | 2 |   |
| 46 |             | VCC      | +3.3V Power                   | 2 |   |
| 47 | LVCMS-I/O   | SCL      | 2-wire Serial interface Data  | 3 | 2 |
| 48 |             | GND      | Ground                        | 1 | 1 |
| 49 | CML-I       | Tx7n     | Transmitter Data Inverted     | 3 |   |
| 50 | CML-I       | Tx7p     | Transmitter Data Non-Inverted | 3 |   |
| 51 |             | GND      | Ground                        | 1 | 1 |
| 52 | CML-I       | Tx5n     | Transmitter Data Inverted     | 3 |   |
| 53 | CML-I       | Tx5p     | Transmitter Data Non-Inverted | 3 |   |
| 54 |             | GND      | Ground                        | 1 | 1 |
| 55 | CML-I       | Tx3n     | Transmitter Data Inverted     | 3 |   |
| 56 | CML-I       | Tx3p     | Transmitter Data Non-Inverted | 3 |   |
| 57 |             | GND      | Ground                        | 1 | 1 |
| 58 | CML-I       | Tx1n     | Transmitter Data Inverted     | 3 |   |
| 59 | CML-I       | Tx1p     | Transmitter Data Non-Inverted | 3 |   |
| 60 |             | GND      | Ground                        | 1 | 1 |

1: OSFP uses common ground (GND) for all signals and supply (power). All are common within the OSFP module and all module voltages are referenced to this potential unless otherwise noted.

2: Open-Drain with pull up resistor on Host.

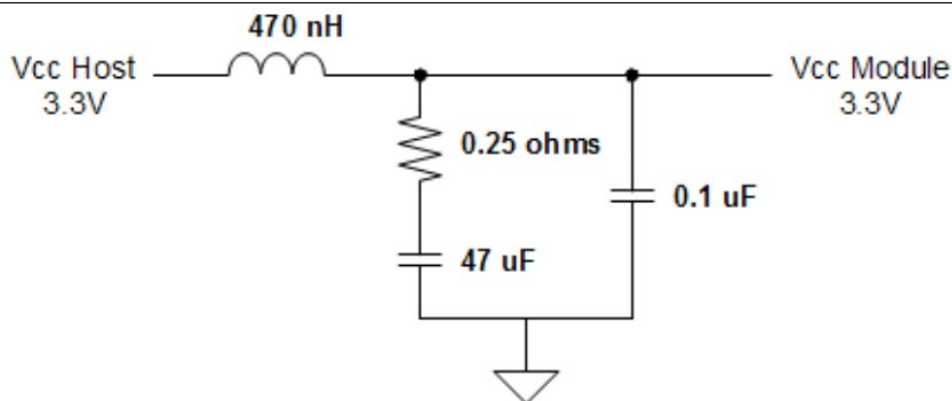


Figure 7: Recommended Host Board Power Supply Filter

For safety and protection of the host system, the power to each OSFP module may be protected by an electronic circuit breaker on the host board which is enabled with the H\_PRSn signal such that power is only enabled when the module is fully engaged into the OSFP connector.

## Package Outline

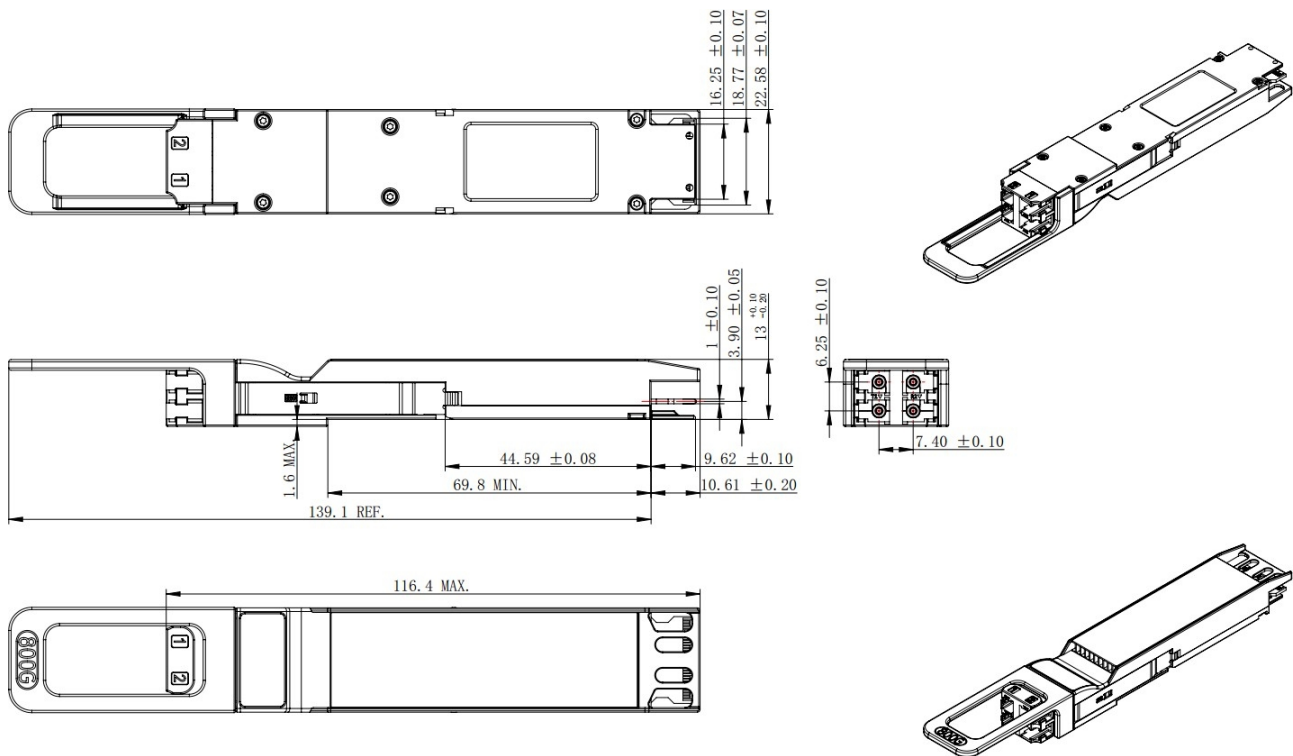


Figure 8: Mechanical Package Outline (All dimensions in mm)

The bellow picture shows the location of the hottest spot for measuring module case temperature. In addition, the digital diagnostic monitors (DDM) temperature is also calibrated to this spot.

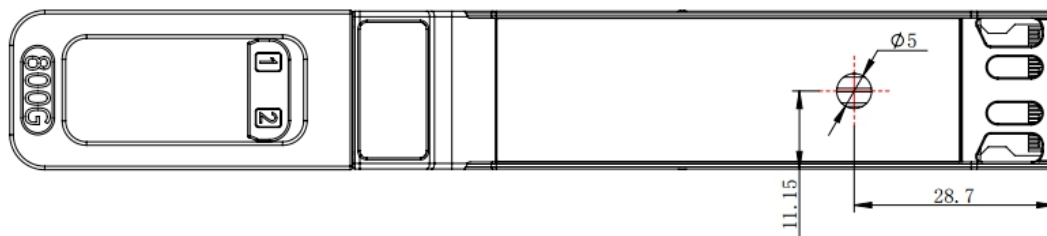


Figure 9: Case Temperature Measurement Point (All dimensions in mm)

\*This 2D drawing is only for reference, please check with Do-Networks before ordering.

The optical interface port is a Dual LC connector.

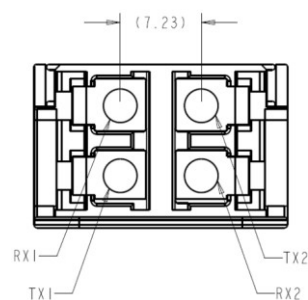


Figure 10: Module Optical Interface (looking into the optical port)

## Control Interface & Memory Map

The control interface combines dedicated signal lines for LPWn/PRSn, INT/RSTn with two-wire serial (TWS), interface clock (SCL) and data (SDA), signals to provide users rich functionality over an efficient and easily used interface.

### SCL and SDA

SCL and SDA are a 2-wire serial interface between the host and module using the I2C or I3C protocols. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value shall be 1k ohms to 4.7k ohms depending on capacitive load.

This 2-wire interface supports bus speeds:

- Required - I2C Fast-mode (Fm)  $\leq 400$  kbit/s
- Optional - I2C Fast-mode Plus (Fm+)  $\leq 1$  Mbit/s
- Optional - I3C Single Data Rate (SDR)  $\leq 12.5$  Mbit/s

The host shall default to using 100 kbit/s standard-mode I2C when first accessing an unidentified module for backward compatibility. Once the module has been brought out of reset, the host can read the module's 2-wire interface speed register to determine the maximum supported speed the module allows. For an OSFP, the host may then use I2C Fast-mode, I2C Fast-mode Plus or I3C Single Data Rate, as indicated by the module. It is optional for the host to change the speed of the 2-wire interface but remaining at a low speed could lead to slow management transactions for modules that require frequent accesses.

SCL and SDA signals follow the electrical specifications of Fast-mode, and Fast-mode Plus as defined in the I2C -bus specification or Single Data Rate mode as defined in the Specification for I3C.

### SCL and SDA Pin Electrical Specifications

| Parameter   | Symbol | Min.    | Typical | Max.    | Unit |
|-------------|--------|---------|---------|---------|------|
| SCL and SDA | VOL    | 0       |         | 0.4     | V    |
|             | VOH    | VCC-0.5 |         | VCC+0.3 | V    |
| SCL and SDA | VIL    | -0.3    |         | VCC*0.3 | V    |
|             | VIH    | VCC*0.7 |         | VCC+0.5 | V    |

### INT/RSTn

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. The circuit shown in OSFP MSA enables multi-level signaling to provide direct signal control in both directions. Reset is an active low signal on the host which is translated to an active-low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active-low signal on the host.

The INT/RSTn signal operates in 3 voltage zones to indicate the state of Reset for the module and Interrupt for the host. Figure 11 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H\_INTn signal and the module uses a voltage reference at 1.25V to determine

the state of the M\_RSTn signal.

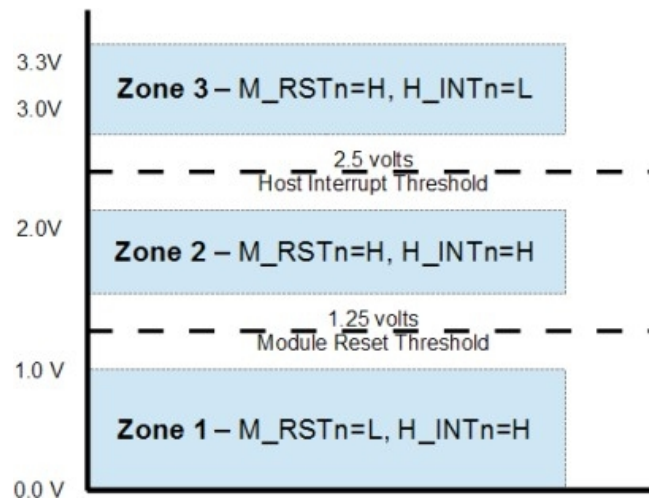


Figure 11: INT/RSTn Voltage Zones

## LPWn/PRSn

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. The circuit shown in OSFP MSA enables multi-level signaling to provide direct signal control in both directions. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.

The LPWn/PRSn signal operates in 3 voltage zones to indicate the state of Low Power mode for the module and Module Present for the host. Figure 12 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H\_PRSn signal and the module uses a voltage reference at 1.25V to determine the state of the M\_LPWn signal.

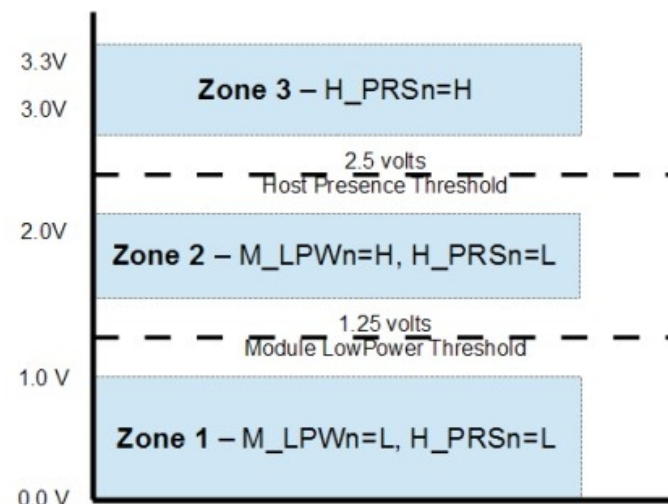


Figure 12: LPWn/PRSn Voltage Zones

## Memory Map

The control interface and memory map of the OSFP module is compliant with the OSFP MSA. The OSFP module support I2C interface protocol defined by the OSFP MSA. Access clock frequency support a

minimum of 100 kHz with no clock stretching and burst read/write of at least 32 bytes.

The module meets the following requirements:

1. The module initialize in hardware mode when LPWn is de-asserted.
2. The transmitter is disabled when the module is held in reset.
3. Tx Squelch function is implemented as defined by the OSFP MSA. When squelched, the transmitter remains on with the modulation turned off.
4. Rx Squelch function is implemented as defined by the OSFP MSA. When Rx CDR LOS is asserted, CDR output is squelched.

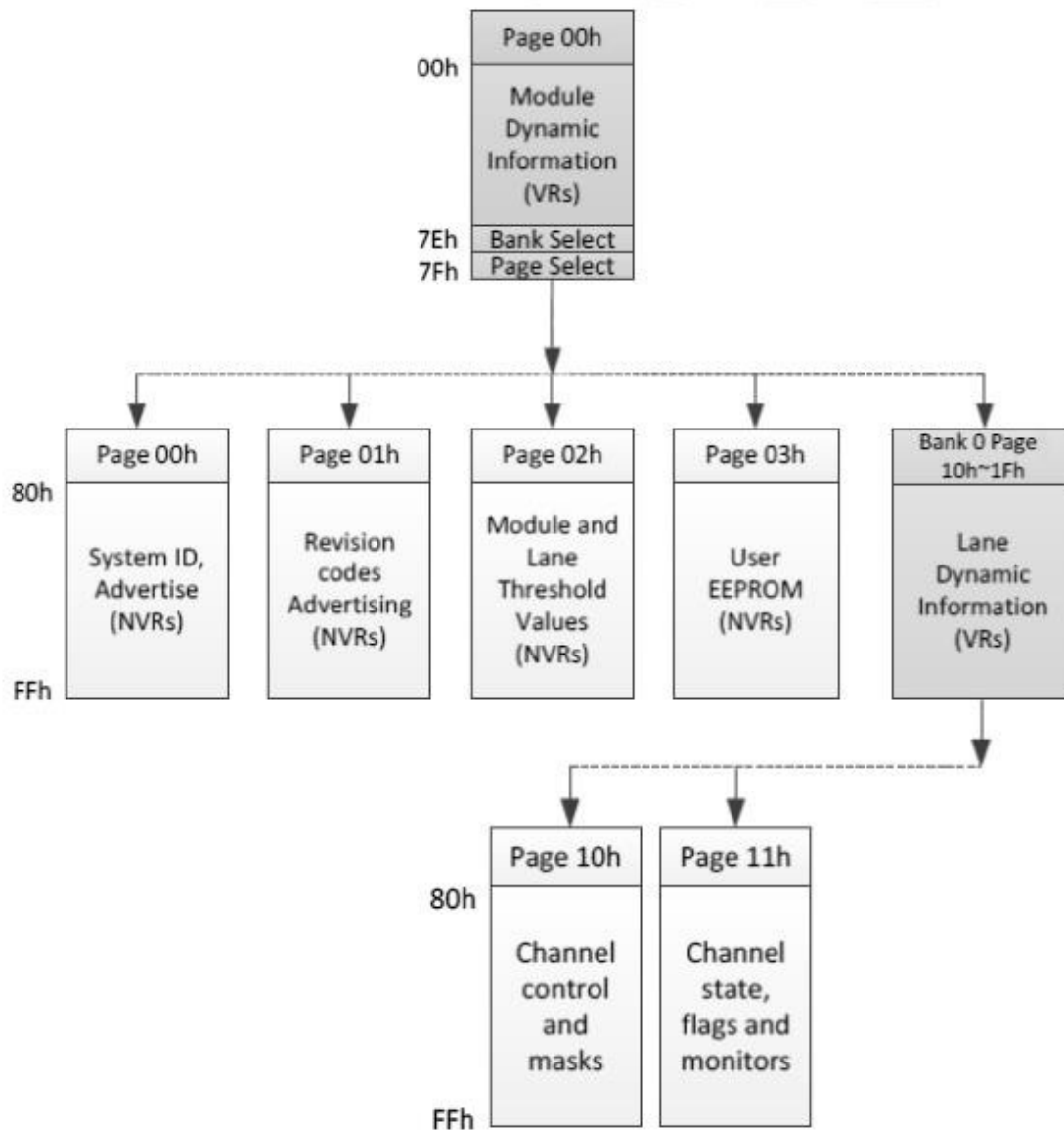


Figure 13: Simplified OSFP CMIS Module Memory Map Architecture

## Revision History

| Revision | Initiated    | Reviewed               | Approved | Revision History | Release Date |
|----------|--------------|------------------------|----------|------------------|--------------|
| V1.a     | Eliss/Julian | Zaki/Nineteen/<br>Viny | Erik     | Released.        | Dec 28, 2023 |

## Quality

Do-Networks Technology has passed many quality system verifications, established an internationally standardized quality assurance system and strictly implemented standardized management and control in the course of design, development, production, installation and service. For latest certification/accreditation numbers, please, contact us.



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