Product Description

Do-Networks's QSFP-DD 800G VR8 transceiver module is designed for use in 800 Gigabit Ethernet links over 50m OM4 and 30m OM3 fiber. The module has 8 independent electrical input/output channels operating at 106.25Gbps per channel. This transceiver consists of two transmitter/receiver units, with each operating on 850nm wavelengths. The transmitter path of the module incorporates a PAM4 re-timer ASIC with two 4-channel modulator drivers and 8 modulated lasers. On the receiver path, it consists of 8 photodiodes and two 4-channel TIAs, along with the PAM4 re-timer. The electrical interface of the module is compliant with the 800GAUI-8 interface as defined by IEEE 802.3ck,and compliant with QSFP-DD MSA.

Features

- Supports 850Gbps
- Single 3.3V Power Supply
- Power Dissipation <14W
- RoHS Compliant (Lead-free)
- QSFP-DD MSA Compliant
- 8x53.125GBd (PAM4)Electrical Interface
- MPO-16 Connector APC
- Commercial Case Temperature Range of 0°C to 70°C
- VCSEL Transmitter
- PIN and TIA Array on the Receiver Side
- I2C interface with integrated Digital Diagnostic Monitoring
- Safety Certification: TUV/UL/FDA*1
- RoHS compliant

Applications*1

- 1x800GEthernet
- 2x400G Ethernet
- 4x200G Ethernet
- 8x100G Ethernet

Ordering Information

Part No.	Data Rate	Fiber	Distance	Interface	Temp.	CMIS
QSFP-DD 800G VR8	850Gbps	OM4/OM3	50m/30m	MPO-16 APC	0~70°C	CMIS4.0*2

*1: For more details, please contact with Do-Networks.

*2: CMIS4.0 or later version.

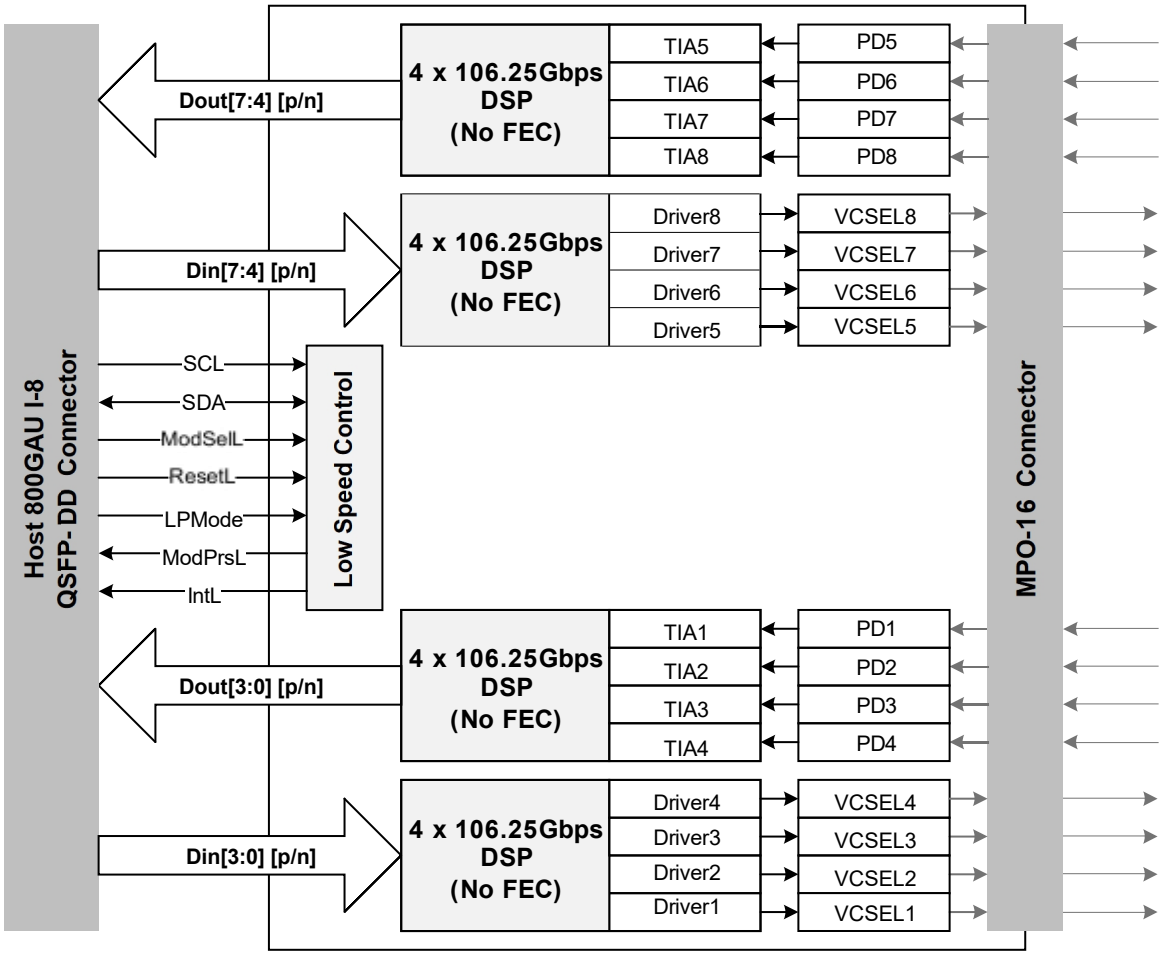


Figure 1: Transceiver Block Diagram

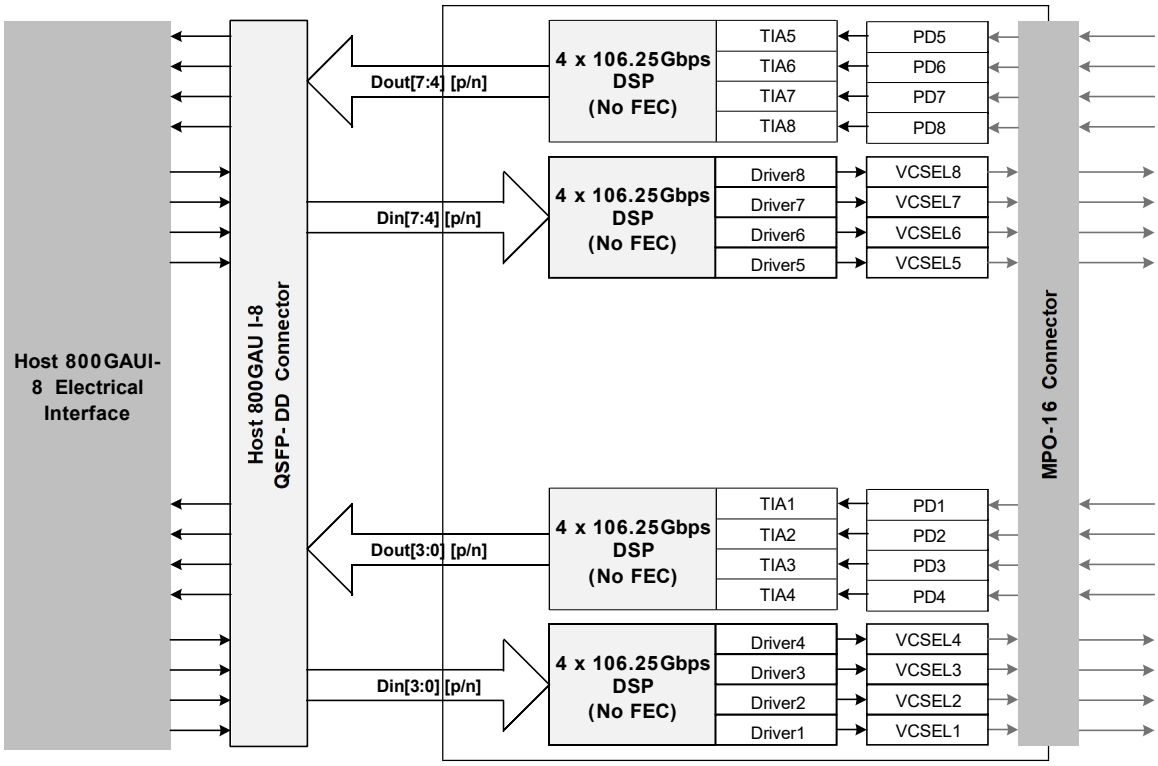


Figure 2: Application Reference Diagram

Transmitter

As shown in Figure 1, the optical transmitter portion of the transceiver incorporates an 8x106.25Gbps 800GAUI-8 electrical input with Equalization (EQ) block, two 4-channel laser drivers and multi-mode laser source. The Tx input buffer provides 800GAUI-8 compliant differential inputs.

Receiver

As shown in Figure 1, the optical receiver portion of the transceiver incorporates eight PIN photodiodes, two 4-channel trans-impedance amplifiers (TIA), integrated 800GAUI-8 compliant electrical output blocks. The Rx output driver provides 800GAUI-8 compliant differential outputs for the high speed electrical interface.

High Speed Electrical Signal Interface

The interface between QSFP-DD module and ASIC/SerDes is shown in Figure 2. The high speed signal lines are internally AC-coupled and the electrical inputs are internally terminated to 100 Ohms differential. All transmitter and receiver electrical channels are compliant to C2M 800GAUI-8 specifications per IEEE 802.3ck.

Control Signal Interface

The following pin is provided to control module or display the module status: ModSelL, ResetL, LPMode, ModPrsL and IntL.In addition, there is an industry standard two wire serial interface scaled for 3.3V LVTTL. The definition of control signal interface and the registers of the serial interface memory are defined in the Control Interface & Memory Map section.

Handling and Cleaning

Exposure to current surges and overvoltage events can cause immediate damage to the transceiver module. Observe the precautions for normal operation of electrostatic discharge sensitive equipment; Attention shall also be paid to limiting transceiver module exposure to conditions beyond those specified in the absolute maximum ratings.
Optical connectors include female connectors. These elements will be exposed as long as the cable or port plug is not inserted. At this time, always pay attention to protection.
Each module is equipped with a port guard plug to protect the optical port. The protective plug shall always be in place whenever the optical fiber is not inserted. Before inserting the optical fiber, it is recommended to clean the end of the optical fiber connector to avoid contamination of the module optical port due to dirty connector. If contamination occurs, use standard MPO port cleaning methods.

Absolute Maximum Ratings*4

Exceeding the absolute maximum ratings table may cause permanent damage to the device. This is just an emphasized rating, and does not involve the functional operation of the device that exceeds the specifications of this technical specification under these or other conditions. Long-term operation under absolute maximum ratings will affect the reliability of the device.

Parameter	Symbol	Min	Typical	Max	Unit
Storage Temperature	Ts	-40		85	°C
3.3 V Power Supply Voltage	Vcc	-0.5	3.3	3.6	V
Relative Humidity (non-condensing)	RH	5		85	%

Recommended Operating Conditions*3

For operations beyond the recommended operating conditions, optical and electrical characteristics are not defined, reliability is not implied, and such operations for a long time may damage the module.

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating case temperature*4	Tc	0		70	°C
Power supply voltage	Vcc	3.135	3.3	3.465	V
Power Supply Noise*5				25	mVpp
Receiver Differential Data Output Load			100		Ohm
Fiber Length (OM4)				50	m
Fiber Length (OM3)				30	m

*3: Power Supply specifications, Instantaneous, sustained and steady state current compliant with QSFP-DD MSA Power Classification.

*4: The position of case temperature measurement is shown in Figure 9.

*5: Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 7 for recommended power supply filter.

General Electrical Characteristics*6

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Symbol	Min.	Typical	Max.	Unit
Transceiver Power Consumption				14	W
Transceiver Power Supply Current, Total				4242	mA
AC coupling capacitors (Internal)			0.1		pF

*6: For control signal timing including ModSelL, ResetL, LPMode, ModPrsL, IntL, SCL and SDA see Control Interface Section.

Reference Points

Test Point	Description
TP1 to TP4	TP1 and TP4 are informative reference points that may be useful to implementers for testing components
TP2	Unless specified otherwise, all transmitter measurements defined in 802.3db167.7 are made at TP2.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 802.3db 167.7 are made at TP3.

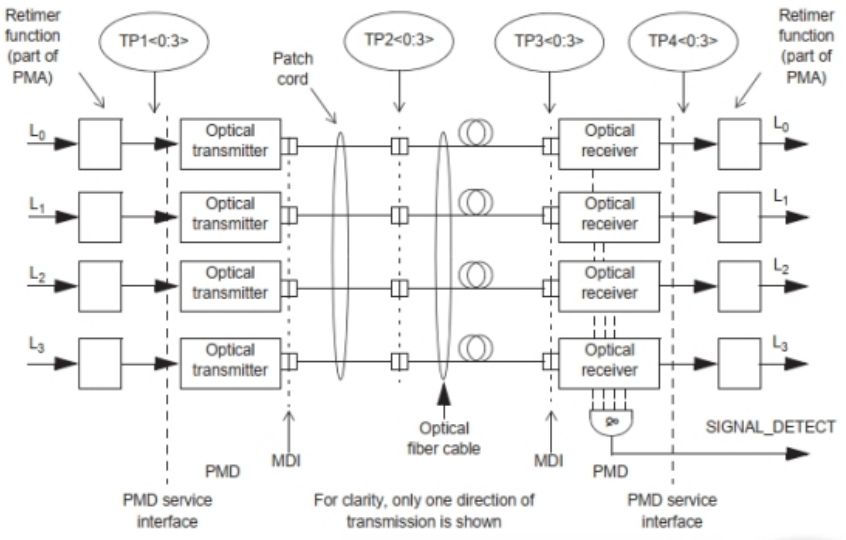


Figure 3: IEEE 802.3db 400GBASE-VR4 or 400GBASE-SR4 transmit/Receive paths

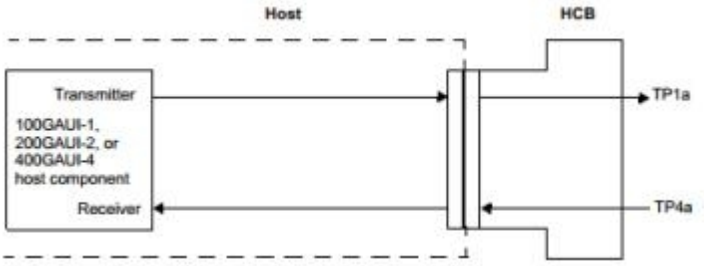


Figure 4: IEEE 802.3ckHost compliance points TP1a, TP4a

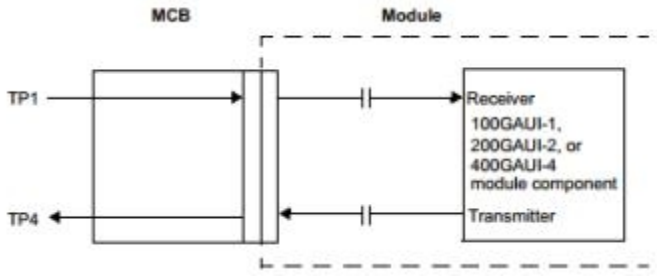


Figure 5: IEEE 802.3ck Module compliance points TP1, TP4

High Speed Electrical Input Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter		Test Point	Min.	Typical	Max.	Unit	Conditions
Signaling rate per lane (range)		TP1		53.125		GBd	+/- 50 ppm
Differential peak-peak input voltage tolerance		TP1a	750			mV	
Peak-to-Peak AC Common-Mode Voltage Tolerance	Low-frequency, VCM_{LF}	TP1a	32			mV	
	Full-band, VCM_{FB}	TP1a	80			mV	
Differential-mode to common-mode return loss		TP1	Equation (120G-2)			dB	
Differential termination mismatch		TP1			10	%	
Single-ended voltage tolerance range		TP1a	-0.4		3.3	V	
DC common-mode voltage tolerance*7		TP1	-350		2850	mV	
Module stressed input test*8		TP1a					
Applied peak-peak sinusoidal jitter				Table 162-17			802.3ck
Eye height (Target)				10		mV	
Vertical eye closure, VEC			12		12.5	dB	

*7: DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

*8:Module stressed input tolerance is measured using the procedure defined in 120G.3.4.3.

High Speed Electrical Output Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Test Point	Min.	Typical	Max.	Unit	Conditions
Signaling rate per lane	TP4		53.125*9		GBd	
AC common-mode output voltage (RMS)	TP4			25	mV	
Differential peak-to-peak output voltage	TP4			600 845	mV	Short mode Long mode
Eye height	TP4	15			mV	
Vertical eye closure, VEC	TP4			12	dB	
Common-mode to differential-mode return loss	TP4	Equation (120G-1)				
Differential termination mismatch	TP4			10	%	
Transition time (20% ~80%)	TP4	8.5			ps	
DC common mode voltage tolerance*10	TP4	-350		2850	mV	

*9: The signaling rate range is derived from the PMD receiver input.

*10: DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

High Speed Optical Transmitter Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Optical Characteristics @TP2 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling rate, each lane	DR	-50ppm	53.125	+50ppm	GBd
Modulation format			PAM4		
Center wavelength	λ	842		868	nm
RMS spectral width*11	△λrms			0.65	nm
Average launch power, each lane*12	Pavg	-4.6		4	dBm
Outer optical modulation amplitude (OMA_{outer}), each lane	Poma			3.5	dBm
Outer optical modulation amplitude (OMA_{outer}), each lane, for max (TECQ,TDECQ)≤1.8dB	Poma	-2.6			dBm
Outer optical modulation amplitude (OMA_{outer}), each lane, for 1.8<max (TECQ,TDECQ)≤4.4dB	Poma	Max (TECQ, TDECQ)-4.4			dBm
Launch power in OMA_{outer} minus TDECQ	OMA-TDECQ	-4.4			dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane	TDECQ			4.4	dB
Transmitter eye closure for PAM4 (TECQ), each lane	TECQ			4.4	dB
Overshoot/undershoot				29	%
Average launch power of OFF transmitter, each lane	Poff			-30	dBm
Extinction ratio, each lane	ER	2.5			dB
$RIN_{14}OMA$	$RIN_{14}OMA$			-132	dB/Hz
Optical return loss tolerance	ORL			14	dB
Encircled flux*14	EF		≥86% at 19 μm ≤30% at 4.5 μm		

*11: RMS spectral width is the standard deviation of the spectrum.

*12: Average launch power, per lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

*13: If measured into type A1a.2 or type A1a.3, or A1a.4, 50um fiber, in accordance with IEC61280-1-4.

High Speed Optical Receiver Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Optical Characteristics @TP3 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling rate, each lane	DR	-50ppm	53.125	+50ppm	GBd
Modulation format			PAM4		
Center wavelength	λ	842		948	nm
Damage threshold*14		5			dBm
Average receiver power, each lane*15		-6.3		4	dBm
Receiver power, each lane (OMA_{outer})				3.5	dBm
Receiver reflectance				-15	dB
LOS Assert	LOSA	-15			dBm
LOS De-Assert	LOSD			-9	dBm
Receiver sensitivity (OMA_{outer}), each lane*16			-4.4 -6.2+TECQ		dBm
Conditions of stressed receiver sensitivity test*17					
Stressed eye closure for PAM4 (SECQ), lane under test			4.4		dB
OMA_{outer} of each aggressor lane			3.5		dBm

*14: The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.

*15: Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

*16: For TECQ≤1.8 dB, the receiver sensitivity OMA (max) should better than-4.4dBm. For 1.8<TECQ≤4.4 dB, the receiver sensitivity OMA (max) should better than-6.2dBm+ TECQ.

*17: These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Regulatory Compliance

Various standard and regulations apply to the QSFP-DD 800G VR8 modules. These include eye-safety, Component Recognition, RoHS, ESD, EMC and Immunity. Please note the transmitter module is a Class 1 laser product. See Regulatory Compliance Table for details.

Regulatory Compliance Table

Feature	Test Method	Performance
Laser Eye Safety and Equipment Type Testing 	(IEC) EN 62368-1:2014+A11 (IEC) EN 60825-1:2014 (IEC) EN 60825-2:2004+A1+A2	CDRH Accession Number:2132182-000 TUV File: R 50457725 0001 CB File: JPTUV-100513
Component Recognition	Underwriters Laboratories (UL) and Canadian Standards Association (CSA) Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File:E317337
RoHS Compliance	RoHS Directive 2011/65/EU& (EU)2015/863	Less than 100 ppm of cadmium. Less than 1000 ppm lead, mercury, hexavalent chromium, poly brominated biphenyls (PPB), poly brominated biphenyl ethers (PBDE),dibutyl phthalate,butyl benzyl phthalate,bis (2-ethylhexyl) phthalate and diisobutyl phthalates.
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM)	High speed contacts shall withstand 1000V. All other contacts shall withstand 2000 V.
Electrostatic Discharge (ESD) to the Optical Connector Receptacle	IEC 61000-4-2:2008	When installed in a properly grounded housing and chassis the units are subjected to 15kV air discharges during operation and 8kV direct discharges to the case.
Electromagnetic Interference (EMI)	FCC Part 15 Class B; CISPR 32 (EN55032) 2015;	System margins are dependent on customer board and chassis design.
Immunity	IEC 61000-4-3:2010; EN55035:2017	Typically shows no measurable effect from a 10V/m field swept from 80 MHz to 6 GHz applied to the module without a chassis enclosure.

Electrostatic Discharge (ESD)

The QSFP-DD 800G VR8 is complying with the ESD requirements described in the Regulatory Compliance Table. However, in the normal processing and operation of optical transceiver, the following two types of situations need special attention.

Case I: Before inserting the transceiver into the rack meeting the requirements of QSFP56 compliant, ESD preventive measures must be taken to protect the equipment . For example, the grounding wrist strap, workbench and floor should be used wherever the transceiver is handled.

Case II: After the transceiver is installed, the electrostatic discharge outside the chassis of the host equipment shall be within the scope of system level ESD requirements. If the optical interface of the transceiver is exposed outside the host equipment cabinet, the transceiver may be subject to equipment system level ESD requirements.

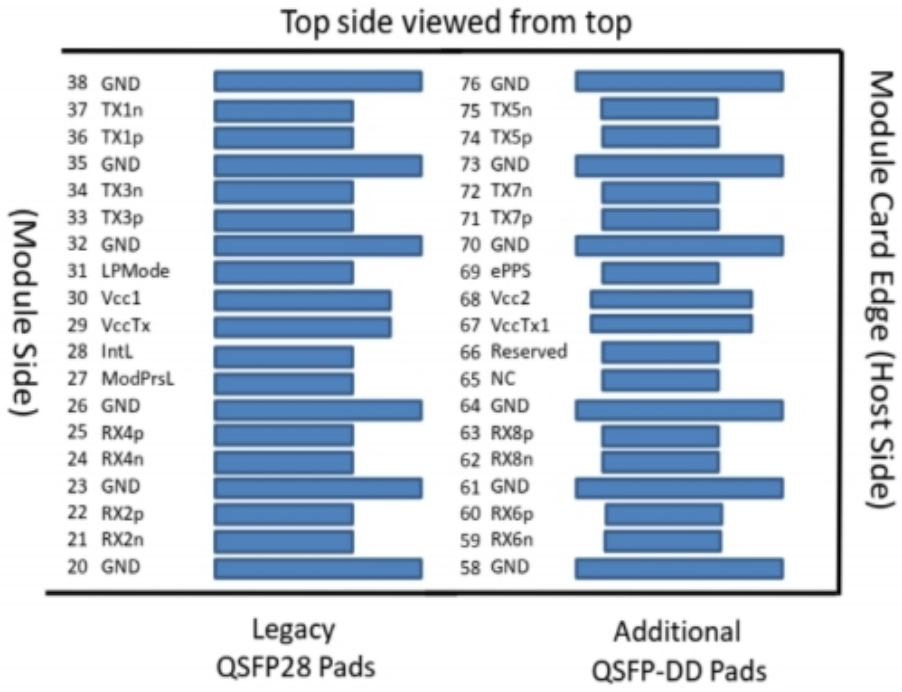
Electromagnetic Interference (EMI)

Communication equipment with optical transceivers is usually regulated by FCC in the United States and CENELEC EN55032 (CISPR 32) in Europe. The compliance of QSFP-DD 800G VR8 with these standards is detailed in the regulatory compliance table. The metal shell and shielding design of QSFP-DD 800G VR8 will help equipment designers minimize the equipment level EMI challenges they face.

Flammability

QSFP-DD 800G VR8optical transceiver meets UL certification requirements, its constituent materials have heat and corrosion resistance, and the plastic parts meet UL94V-0 requirements.

QSFP-DD Transceiver Electrical Pad Layout



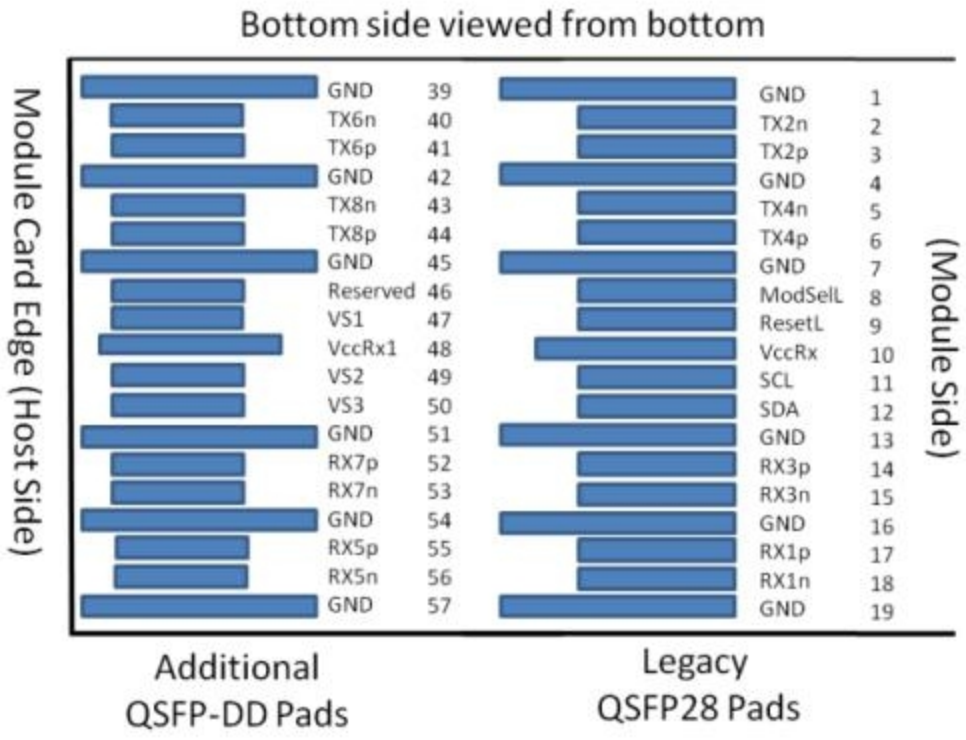


Figure 6: QSFP-DD Module Pinout

Pin Arrangement and Definition

Pin	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS- I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS- I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1

20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power Mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non- Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non- Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	

60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kΩ and less than 100 pF.

4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

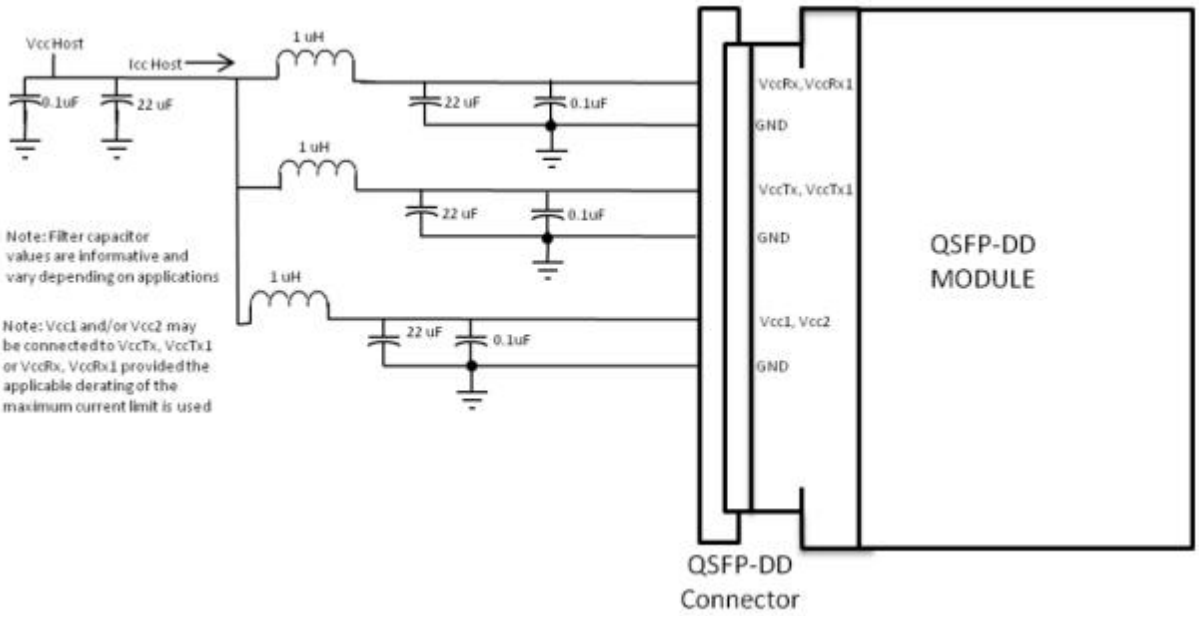


Figure 7: Recommended Host Board Power Supply Filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 Ohm should be used in order to maintain the required voltage at the Host Card Edge Connector. It is recommended that the 22 μF capacitors each have an equivalent series resistance of 0.22 Ohm.

Package Outline

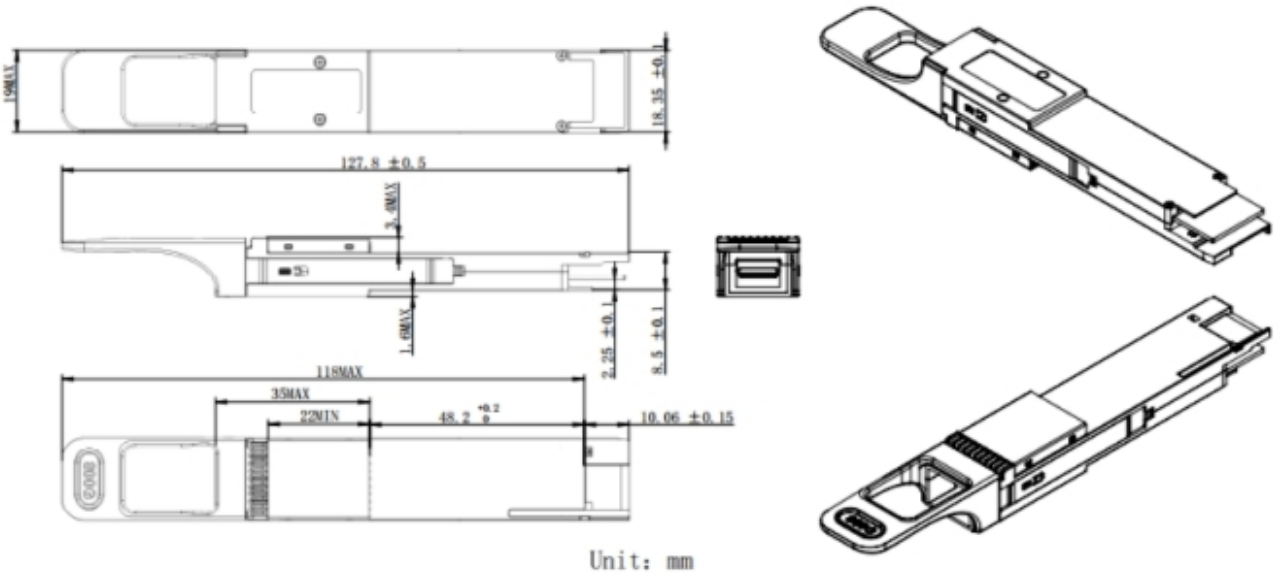


Figure 8: Mechanical Package Outline (All dimensions in mm)

*This 2D drawing is only for reference, please check with Do-Networks before ordering.

The bellow picture shows the location of the hottest spot for measuring module case temperature. In addition, the digital diagnostic monitors (DDM) temperature is also calibrated to this spot.

TBD

Figure 9: Case Temperature Measurement Point (All dimensions in mm)

The optical plug and receptacle for MPO-16 connector is specified in TIA-604-18 and shown in figure 11 (MPO-16 Single Row). Mates with a standard type MPO-16 female plug connector with down-angled interface.

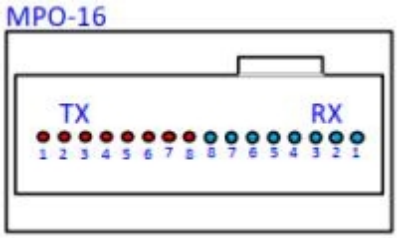


Figure 10: Module Optical Interface (looking into the optical port)

Figure 11: MPO-16 Single Row optical patch cord and module receptacle

Control Interface & Memory Map

The control interface combines dedicated signal lines for ModSelL, ResetL, LPMode, ModPrsL and IntL with two-wire serial (TWS), interface clock (SCL) and data (SDA), signals to provide users rich functionality over an efficient and easily used interface.

SCL and SDA

SCL and SDA are a 2-wire serial interface between the host and module using the I2C protocols. SCL is defined as the serial interface clock signal and SDA as the serialinterface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value shall be 1k ohms to 4.7k ohms depending oncapacitive load.
This 2-wire interface supports bus speeds:

- Required - I2C Fast-mode (Fm) ≤ 400 kbit/s

SCL and SDA Pin Electrical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit
SCL and SDA	VOL	0		0.4	V
	VOH	VCC-0.5		VCC+0.3	V
SCL and SDA	VIL	-0.3		VCC*0.3	V
	VIH	VCC*0.7		VCC+0.5	V

ModSelL

The ModSelL is an input signal that is pulled to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is “High”, the module will not respond to or acknowledge any 2-wire interface communication from the host.
In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL

The ResetL signal is pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state.

LPMode

LPMode is an input signal. The LPMode signal is pulled up to Vcc in the QSFP-DD module. LPMode is used in the control of the module power mode, see CMIS 4.0 Chapter 6.3.1.3.

ModPrsL

ModPrsL shall be pulled up to Vcc Host on the host board and pulled low in the module. The ModPrsL is asserted “Low” when the module is inserted. The ModPrsL is deasserted “High” when the module is physically absent from the host connector due to the pull-up resistor on the host board.

IntL

IntL is an output signal. The IntL signal is an open collector output and shall be pulled to Vcc Host on the host board. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read.

Memory Map

The control interface and memory map of the QSFP-DD module is compliant with the QSFP-DD MSA. The QSFP-DD module supports I2C interface protocol defined by the QSFP-DD MSA. Access clock frequency support a minimum of 100 kHz with no clock stretching and burst read/write of at least 32 bytes.

The module meets the following requirements:

1. The module initialize in hardware mode when LPMode is de-asserted.
2. The transmitter is disabled when the module is held in reset.
3. Tx Squelch function is implemented as defined by the QSFP-DD MSA. When squelched, the transmitter remains off with the modulation turned off.
4. Rx Squelch function is implemented as defined by the QSFP-DD MSA. When Rx CDR LOS is asserted, CDR output is squelched.

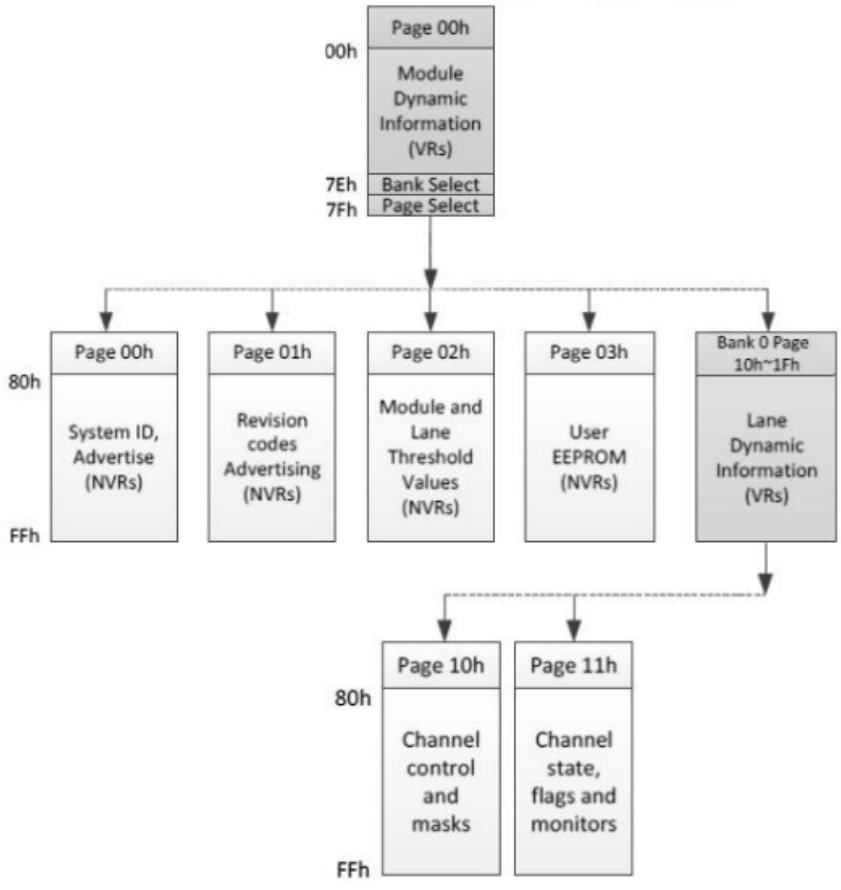


Figure 13: Simplified QSFP-DD CMIS Module Memory Map Architecture .

Revision History

Revision	Initiated	Reviewed	Approved	Revision History	Release Date
V1.a	Roty	Marvin/Jimmy/ Nico/Shawn/Angela	Marvin	Preliminary.	Sep 1,2023

Quality

Do-Networks Technology has passed many quality system verifications, established an internationally standardized quality assurance system and strictly implemented standardized management and control in the course of design, development, production, installation and service. For latest certification/accreditation numbers, please, contactus.

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