Product Description

Do-Networks's OSFP 800G transceiver module is designed for use in 800 Gigabit Ethernet links over 30m OM3 or 50m OM4 fiber. The module has 8 independent electrical input/output channels operating up to 106.25Gbps per channel. This transceiver consists of two transmitter/receiver units, with each operating on 850nm wavelength. The transmitter path of the module incorporates a PAM4 re-timer ASIC with two 4-channel modulator drivers and 8 modulated lasers. On the receiver path, it consists of 8 photodiodes and two 4-channel TIAs, along with the PAM4 re-timer. The electrical interface of the module is compliantwith the 800GAUI-8 interface as defined by IEEE 802.3ck, and compliant with OSFP MSA.

Features

- Supports 850Gbps
- Single 3.3V Power Supply
- Power dissipation < 15W
- 8x53.125GBd (PAM4) Electrical Interface
- Dual MPO-12 Connector APC
- Case Temperature Range: 0°C to 70°C
- VCSEL Transmitter
- PIN and TIA Array on the Receiver Side
- I2C Interface with Integrated Digital Diagnostic Monitoring
- Safety Certification: TUV/UL/FDA*1
- RoHS Compliant
- OSFP MSA Compliant

Applications*1

- 1x800GbE
- 2x400GbE
- 4x200GbE
- 8x100GbE

Ordering Information

Part No.	Data Rate	Fiber	Distance	Interface	DDMI	Structure type	CMIS
800G OSFP112 2xSR4-D	850Gbps	OM3 OM4	60m 100m	Dual MPO-12 APC	Yes	Flat Top	CMIS5.0*2
800G OSFP112 2xSR4-DF	850Gbps	OM3 OM4	60m 100m	Dual MPO-12 APC	Yes	Finned Top	CMIS5.0*2
800G OSFP112 2xSR4-DR	850Gbps	OM3 OM4	60m 100m	Dual MPO-12 APC	Yes	Riding HS	CMIS5.0*2

*1: For more details, please contact with Do-Networks.
*2: CMIS5.0 or later version.
*The product image is only for reference purpose.

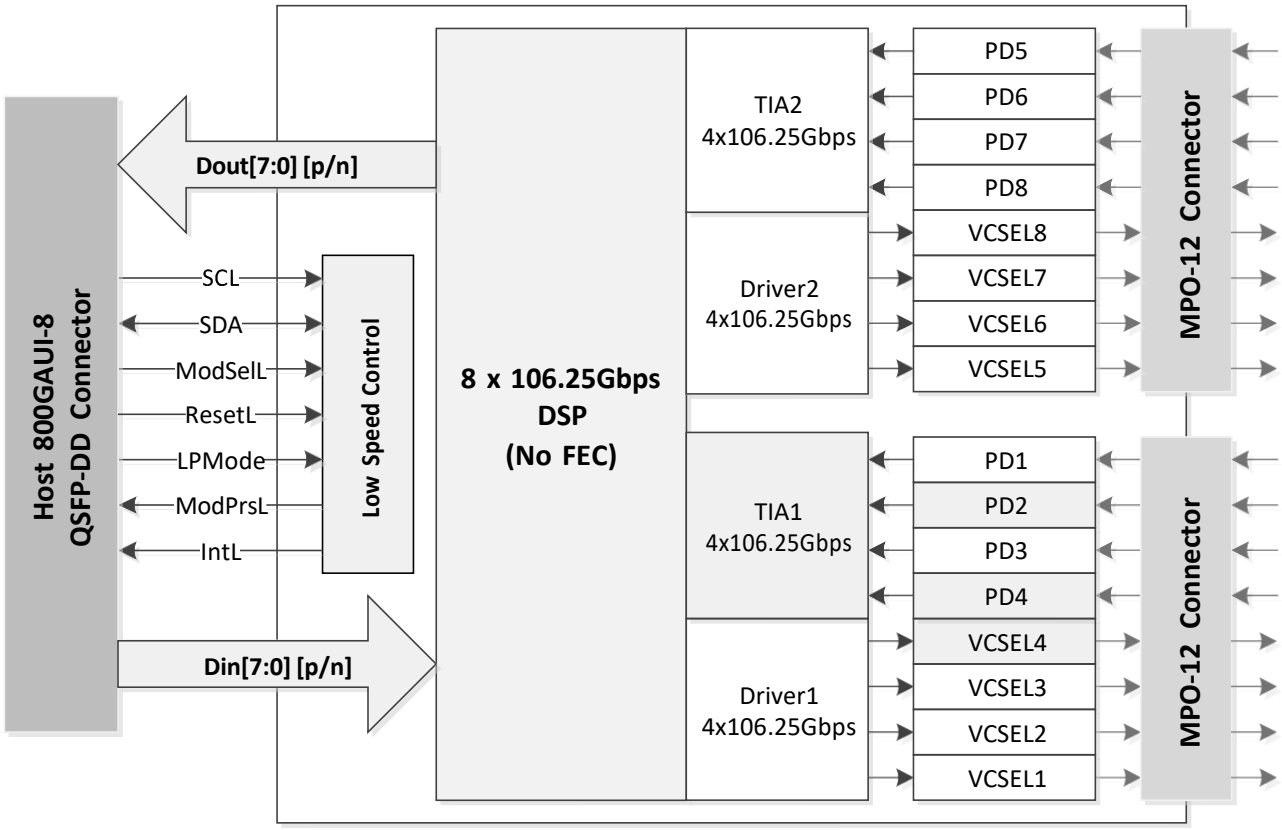


Figure 1: Transceiver Block Diagram

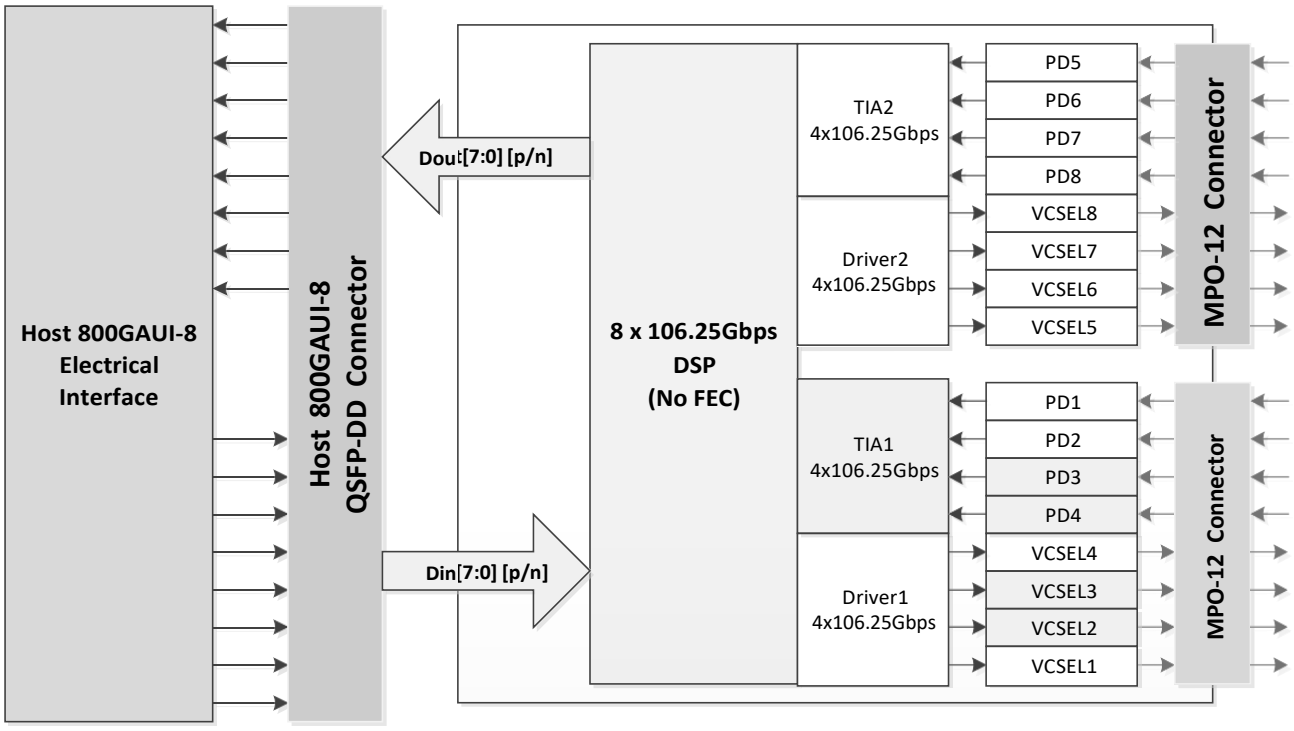


Figure 2: Application Reference Diagram

Transmitter

As shown in Figure 1, the transmitter part of the transceiver contains an 8x106.25Gbps 800GAUI-8 electrical input and equalization (EQ) block, two 4-channel laser drivers and eight multimode laser sources.

Receiver

As shown in Figure 1, the receiver part of the transceiver contains eight PIN photodiodes, two 4-channel trans-impedance amplifiers (TIA) and an integrated 800GAUI-8 compatible electrical output block.

High Speed Electrical Signal Interface

The interface between OSFP module and ASIC/SerDes is showed in Figure 2. The high speed signal lines are internally AC-coupled and the electrical inputs are internally terminated to 100 Ohms differential. All transmitter and receiver electrical channels are compliant to C2M 800GAUI-8 specifications per IEEE 802.3ck.

Control Signal Interface

The control signal interface is compliant with OSFP MSA. The following pin is provided to control module or display the module status: LPWn/PRSn, INT/RSTn. In addition, there is an industry standard two wire serial interface scaled for 3.3V LVTTL. The definition of control signal interface and the registers of the serial interface memory are defined in the Control Interface & Memory Map section.

Handling and Cleaning

Exposure to current surges and overvoltage events can cause immediate damage to the transceiver module. Observe the precautions for normal operation of electrostatic discharge sensitive equipment; Attention shall also be paid to limiting transceiver module exposure to conditions beyond those specified in the absolute maximum ratings.

Optical connectors include female connectors. These elements will be exposed as long as the cable or port plug is not inserted. At this time, always pay attention to protection.

Each module is equipped with a port guard plug to protect the optical port. The protective plug shall always be in place whenever the optical fiber is not inserted. Before inserting the optical fiber, it is recommended to clean the end of the optical fiber connector to avoid contamination of the module optical port due to dirty connector. If contamination occurs, use standard MPO port cleaning methods.

Absolute Maximum Ratings

Exceeding the absolute maximum ratings table may cause permanent damage to the device. This is just an emphasized rating, and does not involve the functional operation of the device that exceeds the specifications of this technical specification under these or other conditions. Long-term operation under absolute maximum ratings will affect the reliability of the device.

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage Temperature	Ts	-40		85	°C
3.3 V Power Supply Voltage	Vcc	-0.5	3.3	3.6	V
Relative Humidity (non-Condensing)	RH	5		85	%

Recommended Operating Conditions*3

For operations beyond the recommended operating conditions, optical and electrical characteristics are not defined, reliability is not implied, and such operations for a long time may damage the module.

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature*4	Tc	0		70	°C
Power Supply Voltage	Vcc	3.135	3.3	3.465	V
Power Supply Noise*5				25	mVpp
Receiver Differential Data Output Load			100		Ohm
Fiber Length (OM3)				30	m
Fiber Length (OM4)				50	m

*3: Power Supply specifications, Instantaneous, sustained and steady state current compliant with QSFP-DD MSA Power Classification.

*4: The position of case temperature measurement is shown in Figure 9.

*5: Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 7 for recommended power supply filter.

General Electrical Characteristics*6

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Symbol	Min.	Typical	Max.	Unit
Transceiver Power Consumption				15	W
Transceiver Power Supply Total Current				4545	mA
AC Coupling Internal Capacitor			0.1		µF

*6: For control signal timing including LPWn/PRSn, INT/RSTn, SCL and SDA see Control Interface Section.

Reference Points

Test Point	Description
TP1 and TP4	TP1 and TP4 are informative reference points that may be useful to implementers for testing components.
TP2	Unless specified otherwise, all transmitter measurements defined in 802.3db 167.7.1 are made at TP2.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 802.3db 167.7.2 are made at TP3.

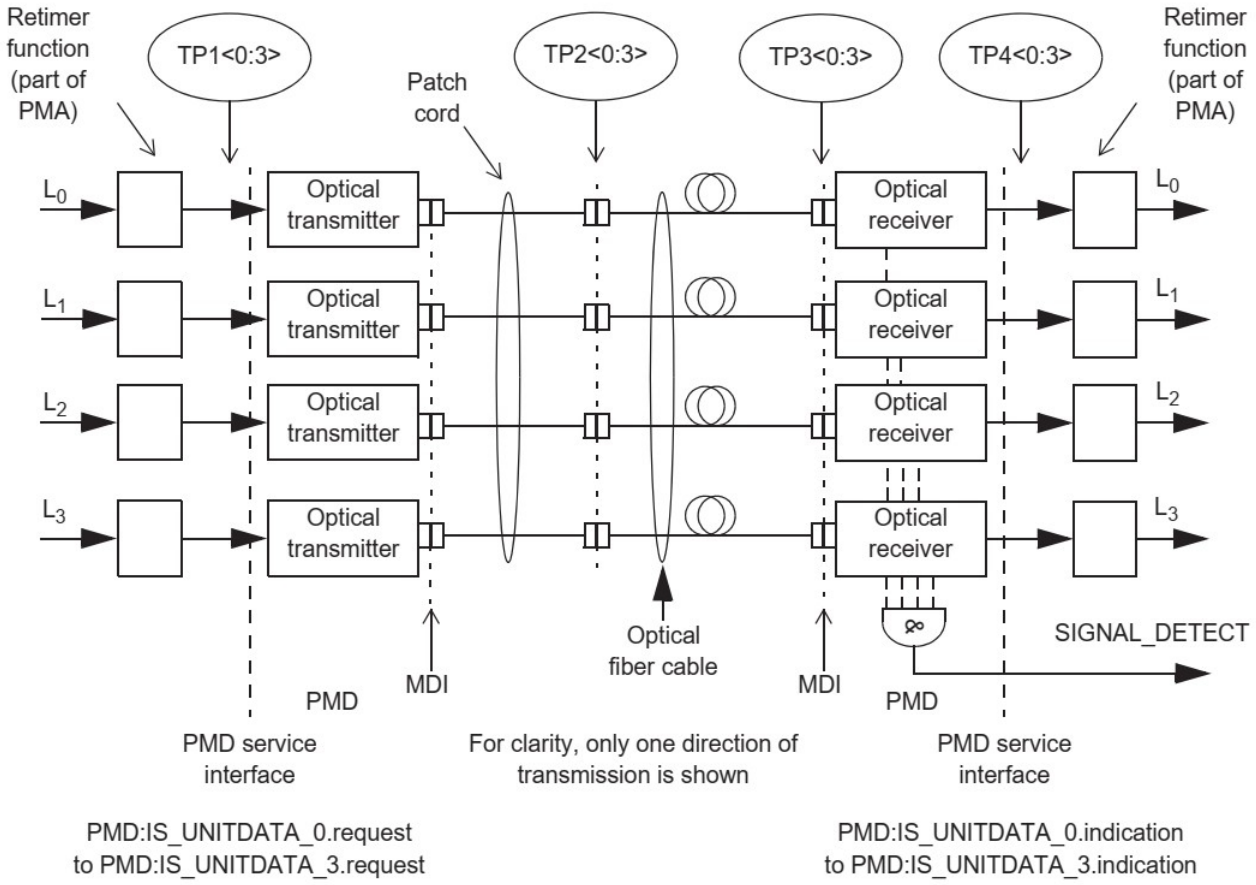


Figure 3: IEEE 802.3db Block Diagram for 400GBASE-VR4 or 400GBASE-SR4 Transmit/Receive Paths

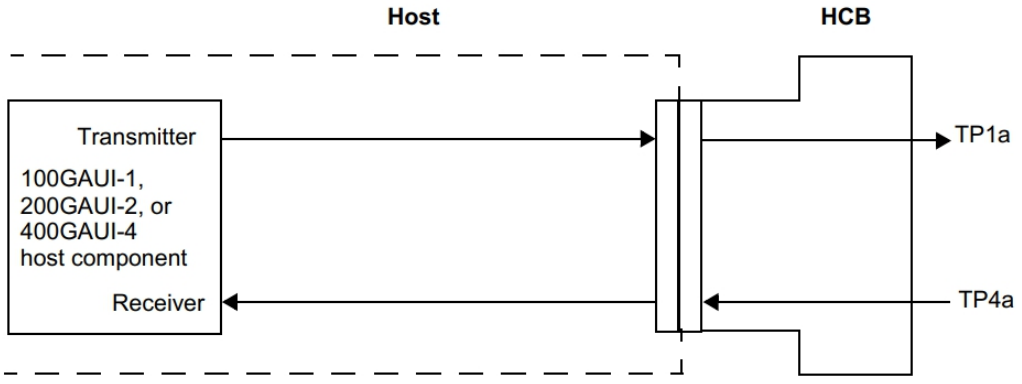


Figure 4: IEEE 802.3ck 400GAUI-4 compliance points TP1a, TP4a

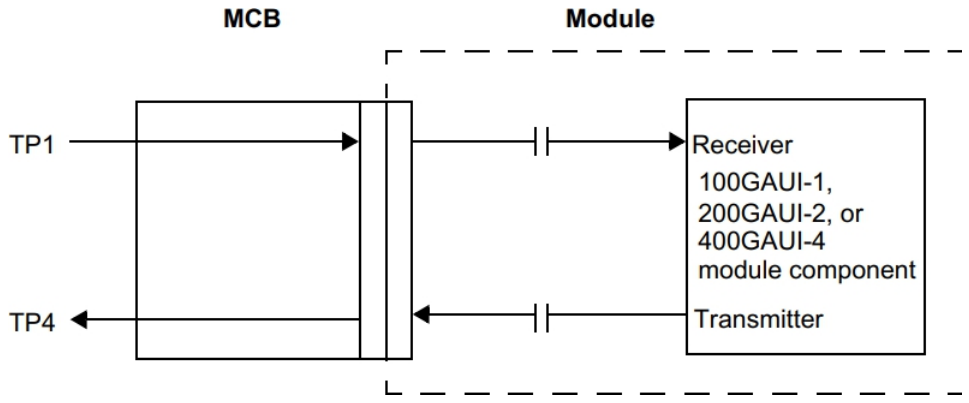


Figure 5: IEEE 802.3ck 400GAUI-4 compliance points TP1, TP4

High Speed Electrical Input Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Test Point	Min.	Typical	Max.	Unit
Signaling Rate per Lane	TP1		53.125± 100ppm		GBd
Differential peak-peak Input Voltage Tolerance*7	TP1a	750			mV
AC Common-Mode RMS Voltage Tolerance	TP1a	25			mV
Differential-Mode to Common-Mode Return Loss, *RLcd*	TP1	Equation (120G-2)*8			dB
Effective Return Loss, *ERL*	TP1	8.5			dB
Differential Termination Mismatch	TP1			10	%
Single-Ended Voltage Tolerance Range	TP1a	-0.4		3.3	V
DC Common-Mode Output Voltage*9	TP1	-350		2850	mV
Module Stressed Input Tolerance*10	TP1a				
Pattern Generator Transition Time (Target)			9		ps
Applied peak-peak Sinusoidal Jitter			Table 162-16*11		
Eye Height (Target)			10		mV
Vertical Eye Closure		12		12.5	dB
Crosstalk Differential peak-peak Voltage			845		mV
Crosstalk Transition Time			8.5		ps

*7: With the exception to 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.

*8: Equation (120G-2) refers to IEEE 803ck.

*9: DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

*10: Meets BER specified in 120G.1.1 of IEEE 802.3ck.

*11: Table 162-16 refers to IEEE 802.3ck.

High Speed Electrical Output Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter		Test Point	Min.	Typical	Max.	Unit
Signaling Rate per Lane		TP4		53.125± 100ppm		GBd
AC Common-Mode Output Voltage (RMS)		TP4			25	mV
Differential Peak-to-Peak Output Voltage	Short Mode				600	mV
		TP4				
	Long Mode				845	mV
Eye Height		TP4	15			mV
Vertical Eye Closure, *VEC*		TP4			12	dB
Common to Differential Mode Conversion Return Loss, *RLdc*		TP4	Equation (120G-1)*12			
Effective Return Loss, *ERL*		TP4	8.5			dB
Differential Termination Mismatch		TP4			10	%
Transition Time (20% ~80%)		TP4	8.5			ps
DC Common Mode Voltage Tolerance*13		TP4	-350		2850	mV

*12: Equation (120G-1) refers to IEEE 802.3ck.

*13: DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

High Speed Optical Transmitter Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Optical Characteristics @TP2 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling Rate, each Lane	DR		53.125± 100ppm		GBd
Modulation Format			PAM4		
Center Wavelength	λ	842		948	nm
RMS Spectral Width*14	oλrms			0.65	nm
Average Launch Power, each Lane	Pavg	-4.6		4	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane (max)	P_{OMA}			3.5	dBm

Outer Optical Modulation Amplitude (OMA_{outer}), each Lane (min) for max (TECQ, TDECQ) ≤1.8dB	P_{OMA}	-2.6		dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane (min) for 1.8<max (TECQ, TDECQ) ≤4.4dB	P_{OMA}	-4.4+max (TECQ, TDECQ)		dBm
Transmitter and Dispersion Eye Closure for PAM4(TDECQ), each Lane	TDECQ		4.4	dB
Overshoot/Undershoot			29	%
Transmitter Power Excursion, each Lane			2.3	dBm
Extinction Ratio, each Lane	ER	2.5		dB
Transmitter Transition Time, each Lane			17	ps
Average Launch Power of OFF Transmitter, each Lane	Poff		-30	dBm
$RIN_{12}OMA$	$RIN_{12}OMA$		-132	dB/Hz
Optical Return Loss Tolerance	ORL		14	dB
Encircled Flux*15	EF	⩾86% at 19 μm ≤30% at 4.5 μm		

*14: RMS spectral width is the standard deviation of the spectrum.

*15: If measured into type A1a.2 or type A1a.3, or A1a.4, 50um fiber, in accordance with IEC61280-1-4.

High Speed Optical Receiver Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Optical Characteristics @TP3 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling Rate, each Lane	DR		53.125± 100ppm		GBd
Modulation Format			PAM4		
Center Wavelength	λ		TBD		nm
Center Wavelength	λ	842		948	nm
Damage Threshold*16		5			dBm
Average Receiver Power, each Lane*17		-6.3		4	dBm
Receiver Power, each Lane (OMA_{outer})				3.5	dBm
Receiver Reflectance				-15	dB
Receiver Sensitivity (OMA_{outer}) for TECQ≤1.8dB	SEN			-4.4	dBm
Receiver Sensitivity (OMA_{outer}) for 1.8<TECQ≤4.4dB	SEN			-6.2+TECQ	dBm
LOS Assert	LOSA	-15			dBm

LOS De-Assert	LOSD	-9	dBm
Stressed Receiver Sensitivity (OMA_{outer}), each Lane*18		-1.8	dBm
Conditions of Stressed Receiver Sensitivity test*19:			
Stressed Eye Closure for PAM4 (SECQ), Lane under Test	4.4		dB
OMA_{outer} of each Aggressor Lane	3.5		dBm

*16: The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.

*17: Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

*18: Measured with conformance test signal at TP3 (see 167.8.14) for the BER specified in 167.1.1.

*19: These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Regulatory Compliance Issues

Various standard and regulations apply to the 800G OSFP112 2xSR4-DX modules. These include eye-safety, Component Recognition, RoHS, ESD, EMC and Immunity. Please note the transmitter module is a Class 1 laser product. See Regulatory Compliance Table for details.

Regulatory Compliance Table

Feature	Test Method	Performance
Laser Eye Safety and Equipment Type Testing 	(IEC) EN 62368-1:2014+A11 (IEC) EN 60825-1:2014 (IEC) EN 60825-2:2004+A1+A2	CDRH Accession Number:2132182-000TUV File: R 50457725 0001 CB File: JPTUV-100513
Component Recognition	Underwriters Laboratories (UL) and Canadian Standards Association (CSA) Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File: E317337
RoHS Compliance	RoHS Directive 2011/65/EU&(EU)2015/863	Less than 100 ppm of cadmium. Less than 1000 ppm lead, mercury, hexavalent chromium, poly brominatedbiphenyls (PPB), poly brominated biphenyl ethers (PBDE), dibutyl phthalate, butyl benzyl phthalate, bis (2-ethylhexyl) phthalate and diisobutyl phthalates.

Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM)	High speed contacts shall withstand 1000V. All other contacts shall withstand 2000 V.
Electrostatic Discharge (ESD)to the Optical Connector Receptacle	IEC 61000-4-2:2008	When installed in a properly grounded housing and chassis the units are subjected to 15kV air discharges during operation and 8kV direct discharges to the case.
Electromagnetic Interference (EMI)	FCC Part 15 Class B; CISPR 32 (EN55032) 2015;	System margins are dependent on customer board and chassis design.
Immunity	IEC 61000-4-3:2010; EN55035:2017	Typically shows no measurable effect from a 10V/m field swept from 80 MHz to 6 GHz applied to the module without a chassis enclosure.

Electrostatic Discharge (ESD)

The 800G OSFP112 2xSR4-DX is complied with the ESD requirements described in the Regulatory Compliance Table. However, in the normal processing and operation of optical transceiver, the following two types of situations need special attention.

Case I: Before inserting the transceiver into the rack meeting the requirements of OSFP compliant cage, ESD preventive measures must be taken to protect the equipment. For example, the grounding wrist strap, workbench and floor should be used wherever the transceiver is handled.

Case II: After the transceiver is installed, the electrostatic discharge outside the chassis of the host equipment shall be within the scope of system level ESD requirements. If the optical interface of the transceiver is exposed outside the host equipment cabinet, the transceiver may be subject to equipment system level ESD requirements.

Electromagnetic Interference (EMI)

Communication equipment with optical transceivers is usually regulated by FCC in the United States and CENELEC EN55032 (CISPR 32) in Europe. The compliance of 800G OSFP112 2xSR4-DX with these standards is detailed in the regulatory compliance table. The metal shell and shielding design of 800G OSFP112 2xSR4-DX will help equipment designers minimize the equipment level EMI challenges they face.

Flammability

800G OSFP112 2xSR4-DX optical transceiver meets UL certification requirements, its constituent materialshave heat and corrosion resistance, and the plastic parts meet UL94V-0 requirements.

OSFP Transceiver Electrical Pad Layout

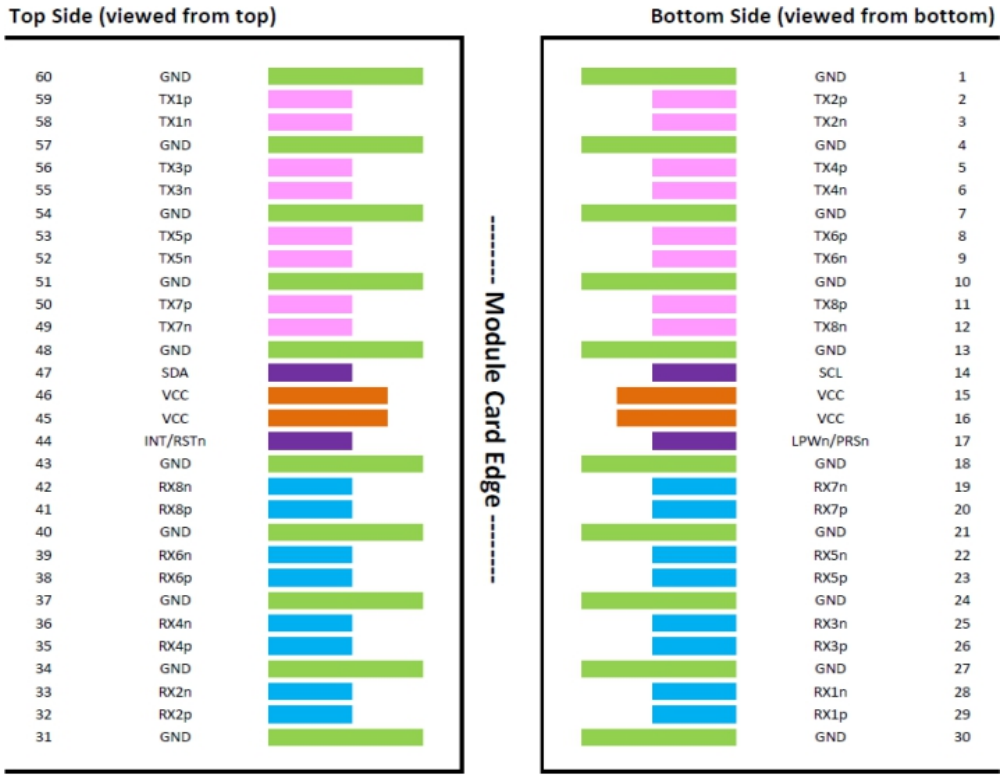


Figure 6: OSFP Module Pinout

Pin Arrangement and Definition

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2p	Transmitter Data Non-Inverted	3	
3	CML-I	Tx2n	Transmitter Data Inverted	3	
4		GND	Ground	1	1
5	CML-I	Tx4p	Transmitter Data Non-Inverted	3	
6	CML-I	Tx4n	Transmitter Data Inverted	3	
7		GND	Ground	1	1
8	CML-I	Tx6p	Transmitter Data Non-Inverted	3	
9	CML-I	Tx6n	Transmitter Data Inverted	3	
10		GND	Ground	1	1
11	CML-I	Tx8p	Transmitter Data Non-Inverted	3	
12	CML-I	Tx8n	Transmitter Data Inverted	3	
13		GND	Ground	1	1
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	3	2
15		VCC	+3.3V Power	2	
16		VCC	+3.3V Power	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present	3	

18		GND	Ground	1	1
19	CML-O	Rx7n	Receiver Data Inverted	3	
20	CML-O	Rx7p	Receiver Data Non-Inverted	3	
21		GND	Ground	1	1
22	CML-O	Rx5n	Receiver Data Inverted	3	
23	CML-O	Rx5p	Receiver Data Non-Inverted	3	
24		GND	Ground	1	1
25	CML-O	Rx3n	Receiver Data Inverted	3	
26	CML-O	Rx3p	Receiver Data Non-Inverted	3	
27		GND	Ground	1	1
28	CML-O	Rx1n	Receiver Data Inverted	3	
29	CML-O	Rx1p	Receiver Data Non-Inverted	3	
30		GND	Ground	1	1
31		GND	Ground	1	1
32	CML-O	Rx2p	Receiver Data Non-Inverted	3	
33	CML-O	Rx2n	Receiver Data Inverted	3	
34		GND	Ground	1	1
35	CML-O	Rx4p	Receiver Data Non-Inverted	3	
36	CML-O	Rx4n	Receiver Data Inverted	3	
37		GND	Ground	1	1
38	CML-O	Rx6p	Receiver Data Non-Inverted	3	
39	CML-O	Rx6n	Receiver Data Inverted	3	
40		GND	Ground	1	1
41	CML-O	Rx8p	Receiver Data Non-Inverted	3	
42	CML-O	Rx8n	Receiver Data Inverted	3	
43		GND	Ground	1	1
44	Multi-Level	INT/RSTn	Module input/Module Reset	3	
45		VCC	+3.3V Power	2	
46		VCC	+3.3V Power	2	
47	LVCMOS-I/O	SCL	2-wire Serial interface Data	3	2
48		GND	Ground	1	1
49	CML-I	Tx7n	Transmitter Data Inverted	3	
50	CML-I	Tx7p	Transmitter Data Non-Inverted	3	
51		GND	Ground	1	1
52	CML-I	Tx5n	Transmitter Data Inverted	3	
53	CML-I	Tx5p	Transmitter Data Non-Inverted	3	
54		GND	Ground	1	1
55	CML-I	Tx3n	Transmitter Data Inverted	3	
56	CML-I	Tx3p	Transmitter Data Non-Inverted	3	
57		GND	Ground	1	1
58	CML-I	Tx1n	Transmitter Data Inverted	3	
59	CML-I	Tx1p	Transmitter Data Non-Inverted	3	
60		GND	Ground	1	1
1: OSFP uses common ground (GND) for all signals and supply (power). All are common within the OSFP					

module and all module voltages are referenced to this potential unless otherwise noted.
2: Open-Drain with pull up resistor on Host.

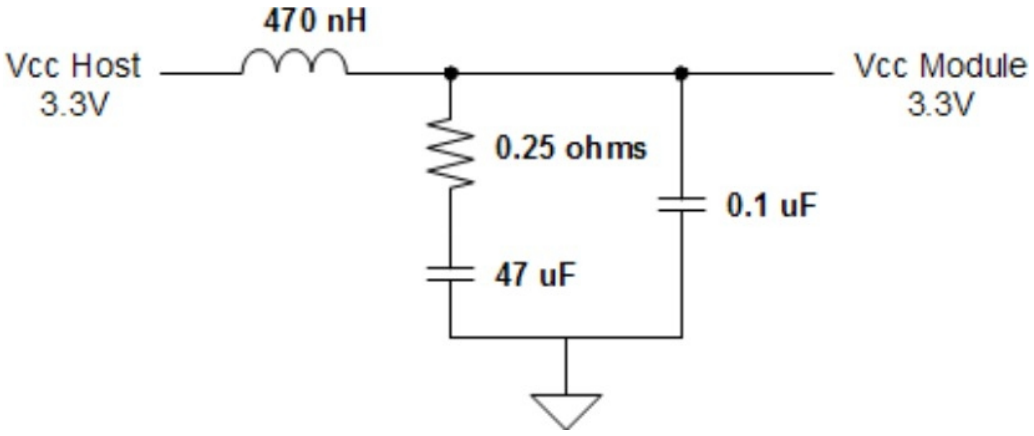
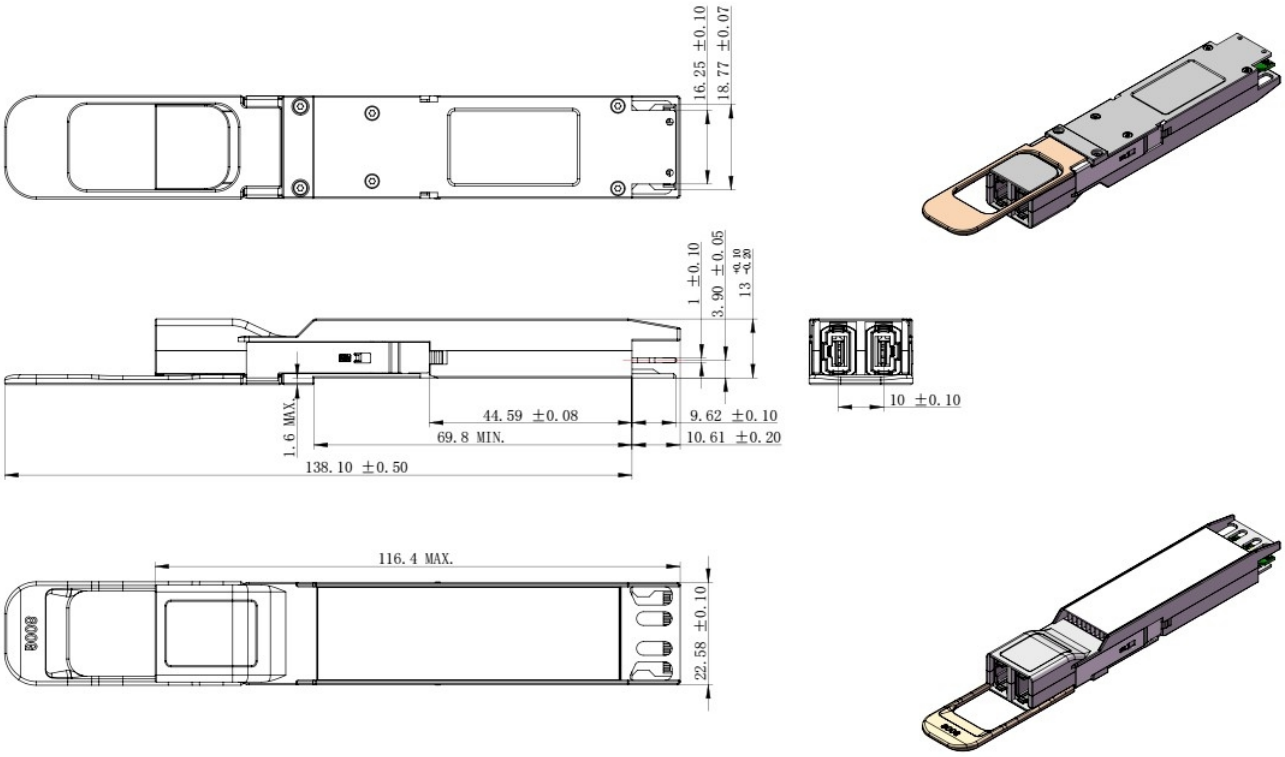


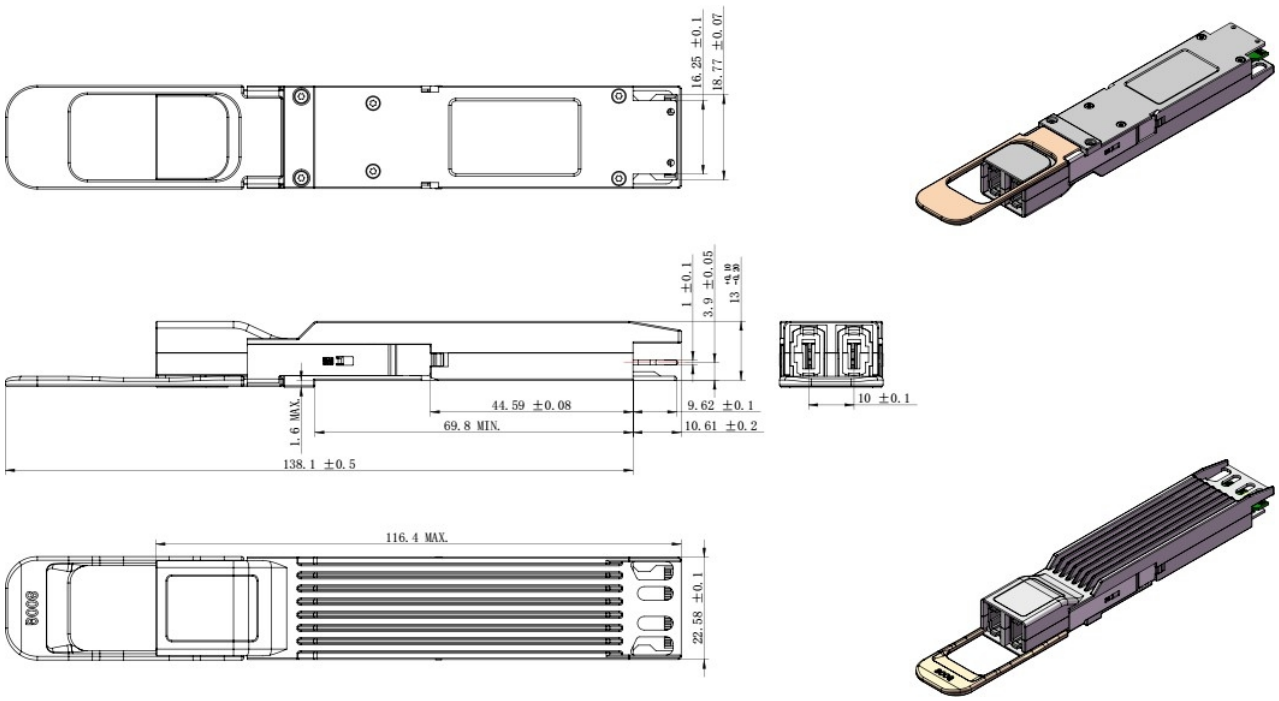
Figure 7: Recommended Host Board Power Supply Filter

For safety and protection of the host system, the power to each OSFP module may be protected by an electronic circuit breaker on the host board which is enabled with the H_PRSn signal such that power is only enabled when the module is fully engaged into the OSFP connector.

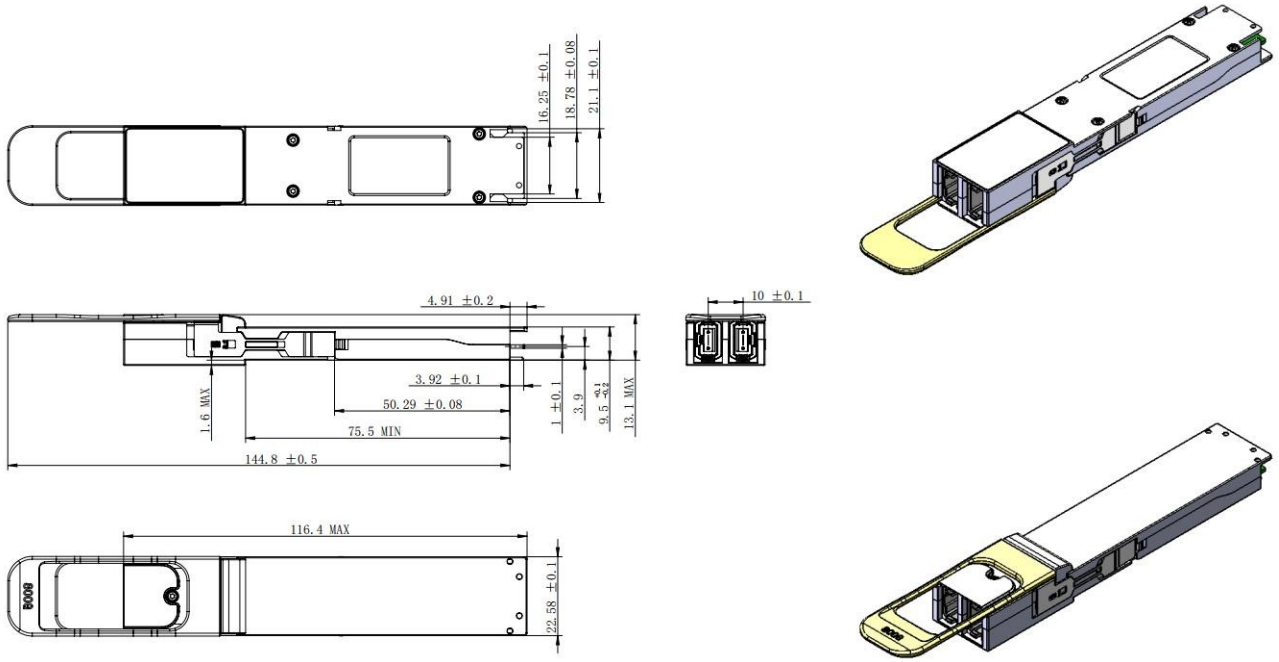
Package Outline



Flat Top



Finned Top



Riding HS

Figure 8: Mechanical Package Outline (All dimensions in mm)

*This 2D drawing is only for reference, please check with Do-Networks before ordering.

The bellow picture shows the location of the hottest spot for measuring module case temperature. Inaddition, the digital diagnostic monitors (DDM) temperature is also calibrated to this spot.

TBD

Figure 9: Case Temperature Measurement Point (All dimensions in mm)

The optical interface port is a male dual MPO-12 connector as specified in IEC 61754-7-1 mates with a standard type MPO-12 female plug connector with down-angled interface.

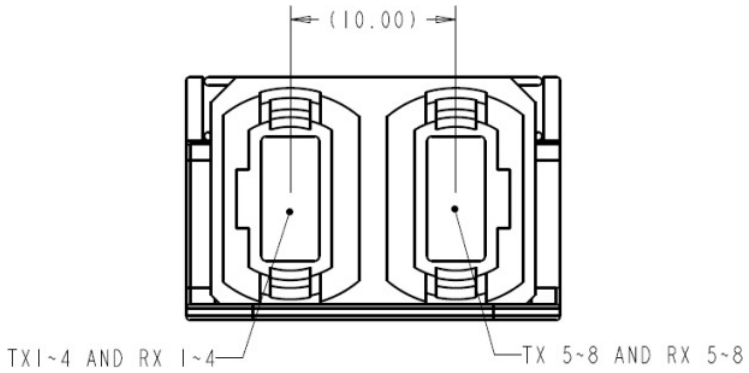


Figure 10: Module Optical Interface (looking into the optical port)

Control Interface & Memory Map

The control interface combines dedicated signal lines for LPWn/PRSn, INT/RSTn with two-wire serial (TWS), interface clock (SCL) and data (SDA), signals to provide users rich functionality over an efficient and easily used interface.

SCL and SDA

SCL and SDA are a 2-wire serial interface between the host and module using the I2C or I3C protocols. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3Von the host. The pull-up resistor value shall be 1k ohms to 4.7k ohms depending on capacitive load.

This 2-wire interface supports bus speeds:

- Required - I2C Fast-mode (Fm) ≤ 400 kbit/s
- Optional - I2C Fast-mode Plus (Fm+) ≤ 1 Mbit/s
- Optional - I3C Single Data Rate (SDR) ≤ 12.5 Mbit/s

The host shall default to using 100 kbit/s standard-mode I2C when first accessing an unidentified module for backward compatibility. Once the module has been brought out of reset, the host can read the module's 2-wire interface speed register to determine the maximum supported speed the module allows. For an OSFP, the host may then use I2C Fast-mode, I2C Fast-mode Plus or I3C Single Data Rate, as indicated by the module. It is optional for the host to change the speed of the 2-wire interface but remaining at a low speed could lead to slow management transactions for modules that require frequent accesses.

SCL and SDA signals follow the electrical specifications of Fast-mode, and Fast-mode Plus as defined in the I2C -bus specification or Single Data Rate mode as defined in the Specification for I3C.

SCL and SDA Pin Electrical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit
SCL and SDA	VOL	0		0.4	V
	VOH	VCC-0.5		VCC+0.3	V
SCL and SDA	VIL	-0.3		VCC*0.3	V
	VIH	VCC*0.7		VCC+0.5	V

INT/RSTn

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. The circuit shown in OSFP MSA Figure11-3 enables multi-level signaling to provide direct signal control in both directions. Reset is an active low signal on the host which is translated to an active-low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active-low signal on the host.

The INT/RSTn signal operates in 3 voltage zones to indicate the state of Reset for the module and Interrupt for the host. Figure 11 shows these 3 zone

s. The host uses a voltage reference at 2.5 volts to determine the state of the H_INTn signal and the module uses a voltage reference at 1.25V to determine the state of the M_RSTn signal.

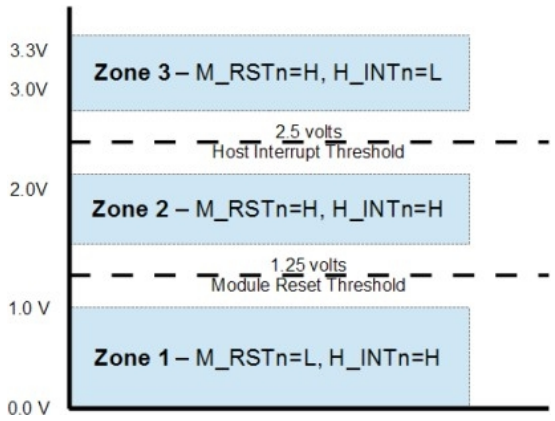


Figure 11: INT/RSTn Voltage Zones

LPWn/PRSn

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. The circuit shown in OSFP MSA Figure11-5 enables multi-level signaling to provide direct signal control in both directions. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.

The LPWn/PRSn signal operates in 3 voltage zones to indicate the state of Low Power mode for the module and Module Present for the host. Figure 12 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_PRSn signal and the module uses a voltage reference at 1.25V to determine the state of the M_LPWn signal.

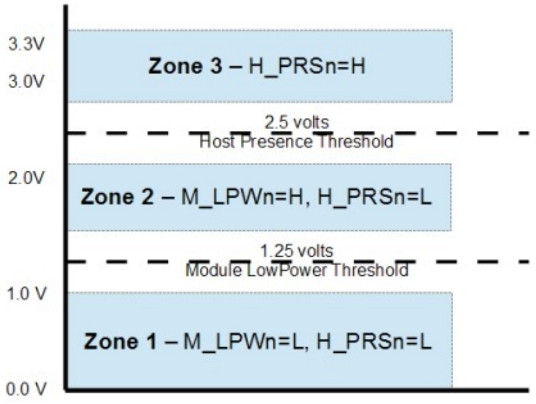


Figure 12: LPWn/PRSn Voltage Zones

Memory Map

The control interface and memory map of the OSFP module is compliant with the QSFP-DD MSA. The OSFP module support I2C interface protocol defined by the QSFP-DD MSA. Access clock frequency support a minimum of 100 kHz with no clock stretching and burst read/write of at least 32 bytes.

The module meets the following requirements:

1. The module initialize in hardware mode when LPWn is de-asserted.
2. The transmitter is disabled when the module is held in reset.
3. Tx Squelch function is implemented as defined by the QSFP-DD MSA. When squelched, the transmitter will be turned off.
4. Rx Squelch function is implemented as defined by the QSFP-DD MSA. When Rx CDR LOS is asserted, CDR output is squelched.

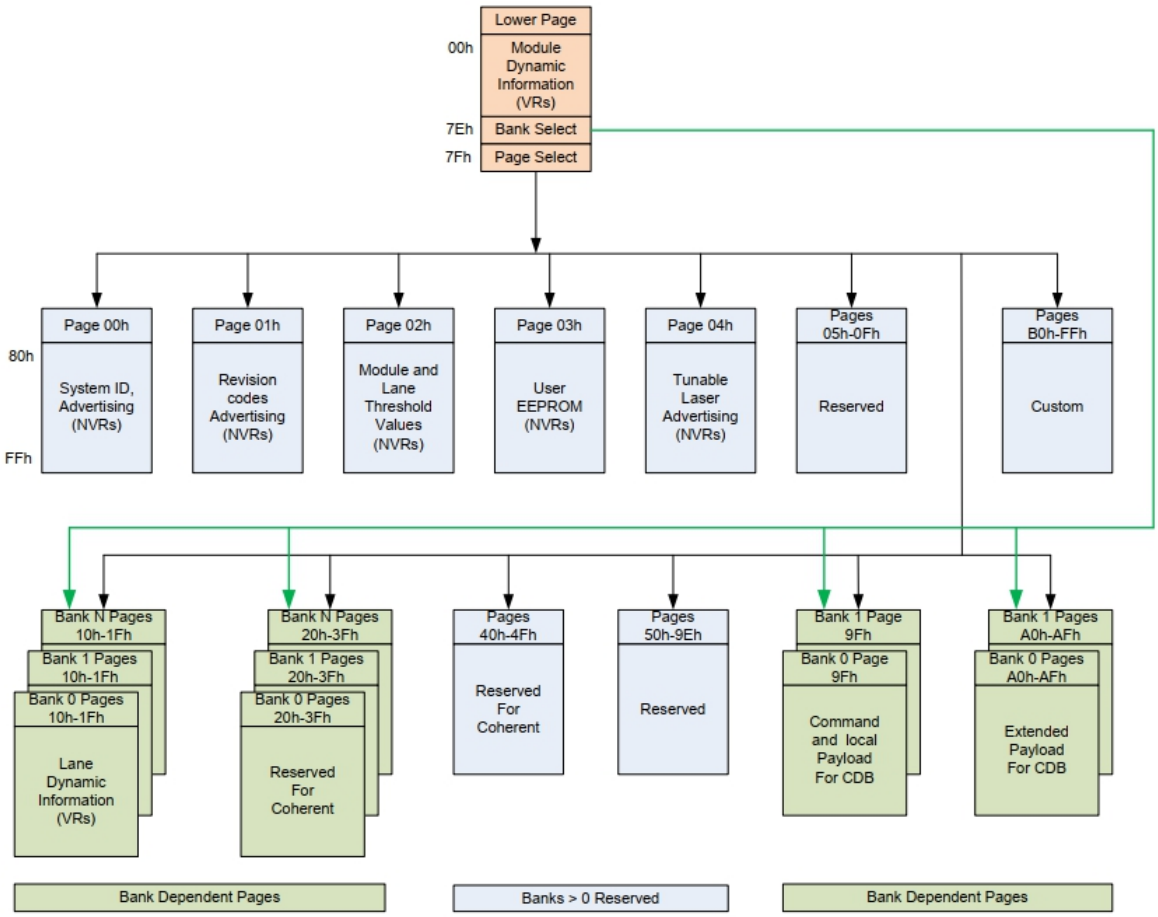


Figure 13: CMIS Module Memory Map

Revision History

Revision	Initiated	Reviewed	Approved	Revision History	Release Date
V1.a	Nico	Marvin/Jimmy/ William/Angela		New Release.	Jul 10, 2023

Quality

Do-Networks Technology has passed many quality system verifications, established an internationally standardized quality assurance system and strictly implemented standardized management and control in the course of design, development, production, installation and service. For latest certification/accreditation numbers, please, contact us.

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