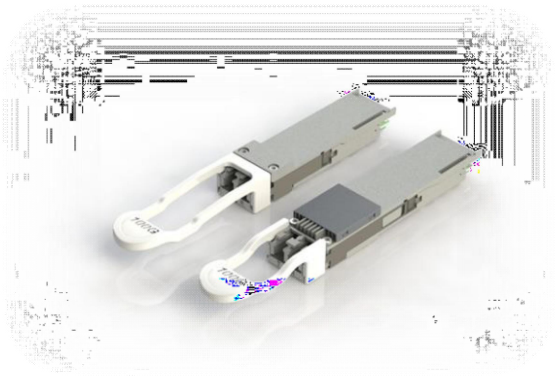
PRELIMINARY Product Specification

High Tx Output Power 100G ZR QSFP28-DCO Transceiver

PRODUCT FEATURES

- Digital Coherent Optics module, hot-pluggable QSFP28 form factor with extended front section outside the cage (cf. QSFP-DD form factor Type 2)
- IEEE 100G Ethernet (CAUI-4) or ITU-T 100G OTN (OTL4.4) compliant host interface
- 100G optical coherent interface with DP-DQPSK modulation and Staircase FEC per IEEE Std. 802.3-2022 100GBASE-ZR or ITU-T G.709.2
- High Tx output power > 0dBm for compatibility with ROADM line systems
- Optional tunable optical filter to suppress out-of-band noise (DOLC3353x3PL1, x = R/S)
- Full C-band tunable, 50GHz or 100GHz grid with optional Flextune™ automatic wavelength tuning
- Case temperature range 0°C to 70°C (C-temp)
- Typical power dissipation < 6.0W
- Remote digital diagnostics monitoring



APPLICATIONS

- Access and aggregation networks
- Cable TV networks
- Wireless mid-haul & back-haul

The DOLC335yx3PL1 (y = 2/3, x = R/S) QSFP28 Digital Coherent Optics (DCO) transceiver supports 100G transmission over distances up to 300km (dispersion limited) for edge network applications. On the host side, the module can accommodate IEEE 100GE Ethernet or ITU-T OTN OTU4 signals. The line side coherent interface specifications are aligned with IEEE Std. 802.3-2022 100GBASE-ZR [9] and ITU-T G.698.2 DW50U-8A2(C)F / DW100U-8A2(C)F [12], which define a 27.95GBd dual-polarization differential QPSK modulation format.

The module has an integrated optical amplifier to enable high Tx output power. Optionally, a Tunable Optical Filter (TOF) is included after the amplifier to suppress out-of-band noise, ensuring compatibility with colorless ROADM line systems. The local oscillator laser is full C-band tunable, and the transceiver can optionally be configured to support Flextune™ automatic wavelength tuning.

The transceiver module is compliant to the Specification for QSFP+ 28 Gb/s 4X Pluggable Transceiver Solution (QSFP28) [1] and specifications referenced therein [2-7], with exceptions for the mechanical dimensions of the front of the transceiver that extends outside the cage, which are aligned with the specifications for the Type 2 QSFP-DD form factor [8]. The transceiver is RoHS compliant as described in Application Note AN-2038 [20-21].

PRODUCT SELECTION

Product	Description
DOLC3352S3PL1	100G ZR QSFP28 Digital Coherent Optics Transceiver, High Tx output power w/o TOF, Fixed grid C-band tunable, 100GE & OTU4, C-temp, 0°C to 70°C, LC receptacle, CMIS
DOLC3353S3PL1	100G ZR QSFP28 Digital Coherent Optics Transceiver, High Tx output power w TOF, Fixed grid C-band tunable, 100GE & OTU4, C-temp, 0°C to 70°C, LC receptacle, CMIS
DOLC3352R3PL1	100G ZR QSFP28 Digital Coherent Optics Transceiver, High Tx output power w/o TOF, Fixed grid C-band tunable, 100GE, C-temp, 0°C to 70°C, LC receptacle, SFF-8636 MIS
DOLC3353R3PL1	100G ZR QSFP28 Digital Coherent Optics Transceiver, High Tx output power w TOF, Fixed grid C-band tunable, 100GE, C-temp, 0°C to 70°C, LC receptacle, SFF-8636 MIS

I. Pin Definitions

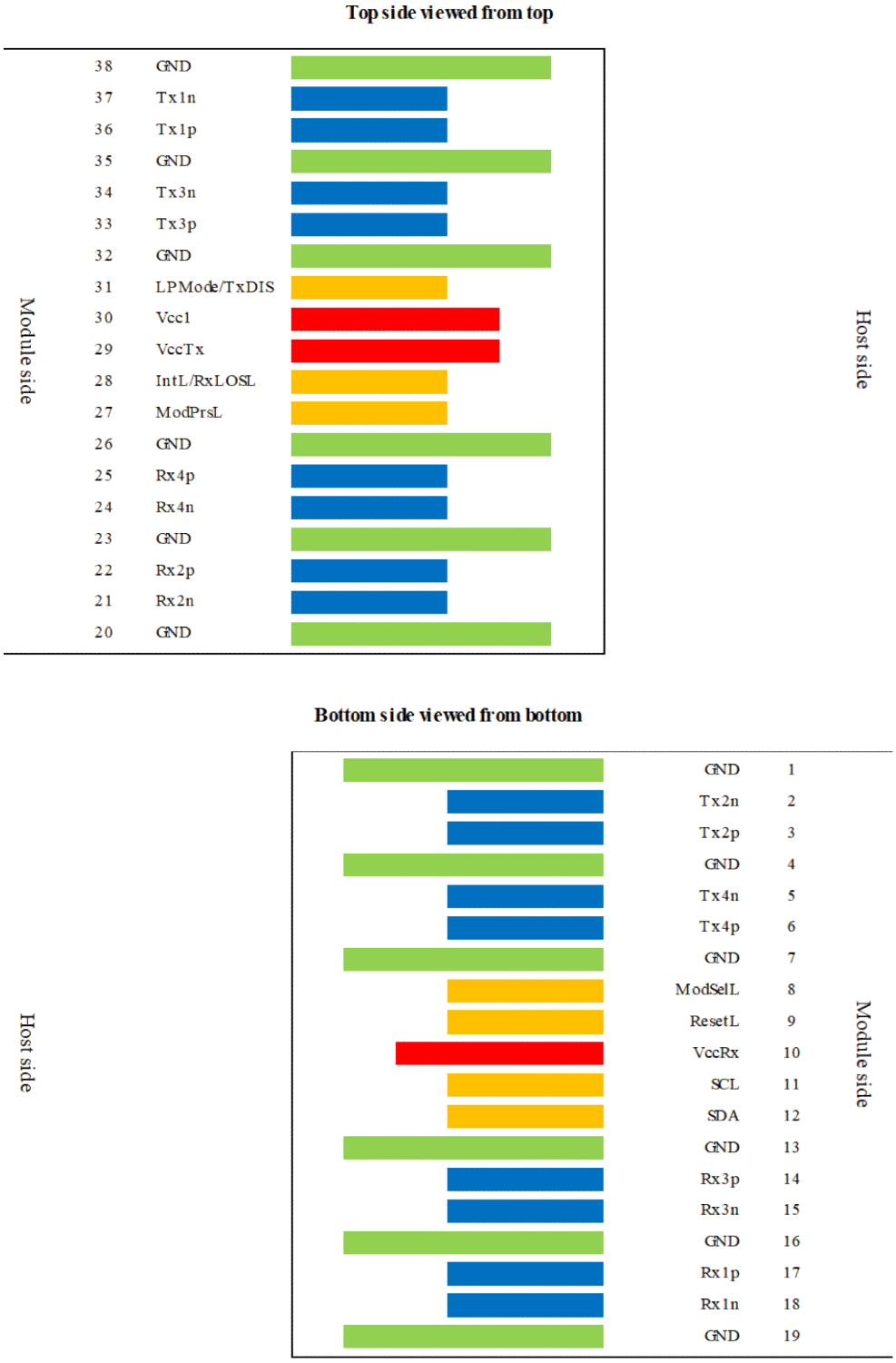


Figure 1 QSFP28-compliant 38-pin connector (per SFF-8679)

Pin	Logic	Symbol	Description	Plug Sequence[3]	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter inverted data input	3	
3	CML-I	Tx2p	Transmitter non-inverted data input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter inverted data input	3	
6	CML-I	Tx4p	Transmitter non-inverted data input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module select	3	
9	LVTTL-I	ResetL	Module reset	3	
10		VccRx	+3.3V power supply receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver non-inverted data output	3	
15	CML-O	Rx3n	Receiver inverted data output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver non-inverted data output	3	
18	CML-O	Rx1n	Receiver inverted data output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver inverted data output	3	
22	CML-O	Rx2p	Receiver non-inverted data output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver inverted data output	3	
25	CML-O	Rx4p	Receiver non-inverted data output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module present	3	
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (CMIS / SFF-8636).	3	
29		VccTx	+3.3V power supply transmitter	2	2
30		Vcc1	+3.3V power supply	2	2
31	LVTTL-I	LPMode/TxDIS	Low power mode. Optionally configurable as TxDis via the management interface (CMIS / SFF-8636).	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter non-inverted data input	3	
34	CML-I	Tx3n	Transmitter inverted data input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter non-inverted data input	3	
37	CML-I	Tx1n	Transmitter inverted data input	3	
38		GND	Ground	1	1

Notes:

1. GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, Vcc1 and VccTx are applied concurrently and may be internally connected within the module in anycombination.
3. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1, 2, 3 (see Figure 1 for pad locations).

II. Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Conditions		Symbol	Min	Typ	Max	Unit	Notes
DC supply voltage			V_{CC}	-0.3		3.6	V	
Low speed I/O voltages				-0.3		3.6	V	
Storage temperature			T_S	-40		85	°C	
Case operating temperature	Central office applications (C-temp)		T_{OP}	-5		75	°C	
Relative humidity	Non-condensing		RH	5		95	%	
Rx input power			$P_{Rx,in}$			10	dBm	
ESD damage threshold	Human body model (HBM)	DC pins		2000			V	
		RF pins		1000				

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

III. Environmental Specifications

Parameter	Conditions		Symbol	Min	Typ	Max	Unit	Notes
Storage temperature			T_S	-40		85	°C	
Case operating temperature	Central office appl. (C-temp)	Long term	T_{OP}	0		70	°C	
		Short term < 96h		-5		75		
Relative humidity	Non-condensing		RH	5		85	%	

IV. Data Path

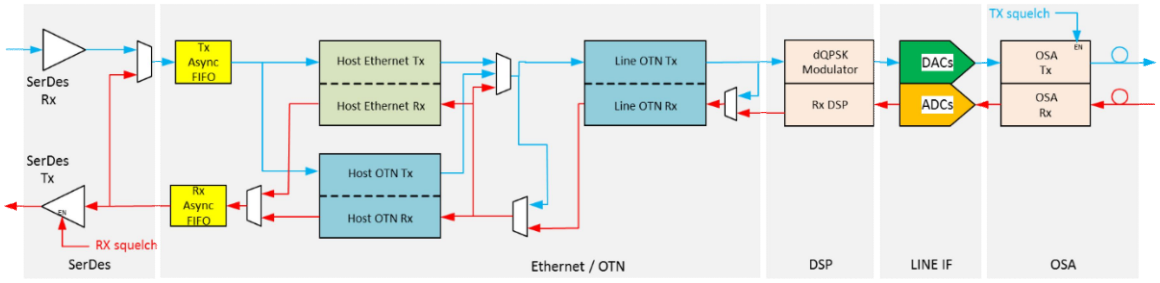


Figure 2 High-level block diagram of DOLC335yx3PL1 (y = 2/3, x = R/S) module data path

A. Host Interface Modes

Host Interface ID [18]	Host Interface Description [18]	Modulation	Forward Error Correction Code	Nominal Symbol Rate (GBd)	Supported Line Interface IDs [18]
DOLC335yS3PL1 and DOLC335yR3PL1					
65 [9]	CAUI-4 C2M without FEC	NRZ	None	25.78125	68, 192, 193
66 [9]	CAUI-4 C2M with RS(528,514) FEC	NRZ	RS(528,514)	25.78125	68, 192, 193
FTLC335yS3PL1 only					
57 [10]	OTL4.4 (ITU-T G.709/ Y.1331 G.Sup58)	NRZ	RS(255,239)	27.9525	192, 193

B. Line Interface Modes

Line Interface ID [18]	Line Interface Description [18]	Modulation	Forward Error Correction Code	Nominal Symbol Rate (GBd)	Spectral Shaping
DOLC335yS3PL1 and DOLC335yR3PL1					
68 [9]	100GBASE-ZR (Clause 154)	DP-DQPSK	Staircase (SC)	27.9525	None
DOLC335yS3PL1 only					
192 [11]	OTU4 Long Reach	DP-DQPSK	Staircase (SC)	27.9525	None
193 [10]	OTU4 Short Reach	DP-DQPSK	RS(255,239)	27.9525	None

C. Data Path Parameters

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Latency							
End-to-end module transit delay	100G DQPSK SC line mode				24	µs	
	100G DQPSK RS line mode				3		
Delay variation	100GE CAUI-4 host mode		-10		10	ns	1
	OTU4 OTL4.4 host mode		-6		6		

Notes:

1. Maximum delay variation for a pair of DOLC3351S3PLt modules over time, including cold restarts, when delay variation is filtered with a low-pass filter with 0.1Hz bandwidth. This is to support transparent transport of IEEE 1588-2019 Precision Time Protocol messages enabling Class C operation.

V. Electrical Characteristics

A. Power & Low Speed I/O

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Power supply - General							
Power supply voltages	Including ripple, droop and noise below 100kHz		3.135	3.300	3.465	V	
Host RMS noise output	10Hz - 10MHz				25	mV	
Module RMS noise output	10Hz - 10MHz				15	mV	
Module supply noise tolerance	10Hz - 10MHz, peak-to-peak	$PSNR_{mod}$			66	mV	
Module inrush	Instantaneous peak duration	T_{ip}			50	µs	
	Initialization time	T_{init}			500	ms	
Power supply - Low power mode							
Power dissipation		P_{lp}			1.5	W	
Power supply current	Instantaneous peak current	$I_{CC,ip,lp}$			600	mA	
	Sustained peak current	$I_{CC,sp,lp}$			495		
	Steady state current	$I_{CC,lp}$			478		1
Power supply - High power mode DOLC335yS3PL1 / DOLC335yR3PL1 – 2.4 ns/nm CD)							
Power dissipation		P_{hp}		5.5	6.2	W	
Power supply current	Instantaneous peak current	$I_{CC,ip,hp}$			2480	mA	
	Sustained peak current	$I_{CC,sp,hp}$			2046		
	Steady state current	$I_{CC,hp}$			1978		1
Power supply - High power mode (DOLC335yS3PL1 – 6.0 ns/nm CD)							
Power dissipation		P_{hp}		5.7	6.5	W	
Power supply current	Instantaneous peak current	$I_{CC,ip,hp}$			2600	mA	
	Sustained peak current	$I_{CC,sp,hp}$			2145		
	Steady state current	$I_{CC,hp}$			2073		1
Low speed I/O							
Clock frequency, SCL	Default	f_{SCL}		400		kHz	
	Fast mode+			1000			
Output voltage, SCL and SDA	Output low	V_{OL}	0.0		0.4	V	
	Output high	V_{OH}	V_{CC}-0.5		V_{CC}+0.3		
Input voltage, SCL and SDA	Input low	V_{IL}	-0.3		0.3×V_{CC}	V	
	Input high	V_{IH}	0.7×V_{CC}		V_{CC}+0.5		
Capacitance for SCL and SDA I/O signal		Ci			14	pF	
Total bus capacitive load for SCL and SDA	400kHz clock rate, 3.0kΩ pull-up resistor, max.	Cb			100	pF	2
	400kHz clock rate, 1.6kΩ pull-up resistor, max.				200		
Input voltage / current, LPMode/TxDis, ResetL and ModSelL	Input voltage, low	V_{IL}	-0.3		0.8	V	
	Input voltage, high	V_{IH}	2.0		V_{CC}+0.3		
	Input current, 0V < V_{in} < V_{CC}	I_{in}	-365		125	µA	
Output voltage, ModPrsL and IntL/RxLOSL	Output low, I_{OL} = 2mA	V_{OL}	0.0		0.4	V	
	Output high, 10kΩ pull-up resistor to host V_{CC}	V_{OH}	V_{CC}-0.5		V_{CC}+0.3		

Notes:
1. The module will stay within its advertised power class for all supply voltages.
2. For 1000kHz clock rate, refer to Figure 6-4 in [2]

B. High Speed Data I/O

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Transmitter (module input) – CAUI-4							
Signaling rate per lane			Per IEEE Std 802.3 [9], Annex 83E, Table 83E–7			GBd	
Differential pk-pk input voltage tolerance						mV	
Differential input return loss						dB	
Differential to common mode input return loss						dB	
Differential termination mismatch						%	
Module stressed input test							
Single-ended voltage tolerance range						V	
DC common mode voltage						mV	
Transmitter (module input) – OTL4.4							
Overload differential voltage pk-pk			Per OIF-CEI-04.0 [15], Clause 13 CEI-28G-VSR, Table 13-2			mV	
Common mode voltage						mV	
Differential termination resistance mismatch						%	
Differential return loss						dB	
Differential mode to common mode conversion						dB	
Stressed input test							
Receiver (module output) – CAUI-4							
Signaling rate per lane			Per IEEE Std 802.3 [9], Annex 83E, Table 83E–3			GBd	
AC common-mode output voltage						mV	
Differential peak-to-peak output voltage						mV	
Eye width						UI	
Eye height, differential						mV	
Vertical eye closure						dB	
Differential output return loss						dB	
Common to differential mode conversion return loss						dB	
Differential termination mismatch						%	
Transition time						ps	
DC common mode voltage						mV	
Receiver (module output) – OTL4.4							
Differential voltage, pk-pk			Per OIF-CEI-04.0 [15], Clause 13 CEI-28G-VSR, Table 13-4			mV	
Common mode voltage						mV	
Common mode noise, RMS						mV	
Differential termination resistance mismatch						%	
Differential return loss						dB	
Common mode to differential mode conversion						dB	
Common mode return loss						dB	
Transition time						ps	
Vertical eye closure						dB	
Eye width						UI	
Eye height						mV	

VI. Optical Characteristics

A. General

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Symbol rate		R_{baud}		27.95		GBd	
Modulation format				DP-DQPSK			
Channel frequency range	100GHz grid	v_C	191.400	193.700	196.100	THz	
	50GHz grid		191.350	193.700	196.100		
Channel spacing	100GHz grid	Δv_C		100		GHz	
	50GHz grid			50			
Frequency accuracy		δv_C	-1.8		1.8	GHz	
Laser intrinsic linewidth	Calculated based on FM noise power spectral density (PSD) measurement	LW			500	kHz	
Side-mode suppression ratio	No modulation	SMSR	40			dB	
Relative intensity noise	Peak over 0.2GHz < f < 10GHz	RIN			-140	dB/Hz	

B. Transmitter

Parameter	Conditions		Symbol	Min	Typ	Max	Unit	Notes
Tx output power			$P_{Tx,out}$	0		-	dBm	
Tx output power monitor range			$P_{Tx,mon}$	-2		4	dBm	
Tx output power monitor accuracy	Tx optical power monitor reading relative to actual Tx output power		$\delta P_{Tx,mon}$	-1.5		1.5	dB	
Tx output power during tuning or when Tx disabled			$P_{Tx,dark}$			-35	dBm	
Tx spectral excursion	ITU-T G.698.2 §7.2.3 [12]			-15		15	GHz	
Tx output power imbalance between X- and Y-polarizations			$\Delta P_{X/Y}$			1.5	dB	
Tx XY skew						6.0	ps	
Tx IQ offset						-25	dB	
Tx IQ imbalance						1.0	dB	
Tx quadrature error				-7.0		7.0	°	
Tx IQ skew						1.5	ps	
Tx error vector magnitude mask ratio	ITU-T G.698.2 §7.2.12 [12], with 24dB/12.5GHz noise loading					23	%	
Tx in-band optical signal to noise ratio	Under modulation, |Δf| < 60 GHz	DOLC3352x3PL1	$OSNR_{in}$	39			dB/ 12.5GHz	
		DOLC3353x3PL1		39				
Tx out-of-band optical signal to noise ratio	Under modulation, |Δf| > 150 GHz	DOLC3352x3PL1	$OSNR_{out}$	30			dB/ 12.5GHz	
		DOLC3353x3PL1		45				
Tx reflectance						-20	dB	

C. Receiver

Parameter	Conditions		Symbol	Min	Typ	Max	Unit	Notes
Rx total input power	Broadband		$P_{Rx,tot}$	-30		3	dBm	
Rx signal input power (amplified)	Full Rx OSNR tolerance		$P_{Rx,sig}$	-18		1	dBm	
	Extended range			-22		3		1
Rx OSNR tolerance	Back-to-back, $P_{Rx,sig}$ > -18dBm	100G DQPSK SC		16.5			dB/ 12.5GHz	2
		100G DQPSK RS		21.5				
CD tolerance	Default, OSNR penalty < 0.5dB					2.4	ns/nm	
	Extended, OSNR penalty < 1.0dB					6.0		3
PMD tolerance	OSNR penalty < 0.5dB					10	ps	
DGD tolerance	OSNR penalty < 0.5dB					30	ps	
Tolerance to change in SOP	OSNR penalty < 0.5dB					50	krad/s	
PDL OSNR penalty	Change in principal state of polarization < 1rad/ms	1dB PDL				0.5	dB/ 12.5GHz	
		2dB PDL				1.0		
		4dB PDL				3.0		
Rx signal input power transient amplitude	Peak excursion from steady state, transient within Rx signal input power (amplified) range, OSNR penalty < 0.5dB			-3		3	dB	
Rx signal input power transient rise/fall time	Rise/fall time for the above peak excursion, OSNR penalty < 0.5dB			100			µs	
Colorless drop OSNR penalty	Rx total input power to signal input power ratio < 12dB					0.5	dB	4
Colorless drop adjacent channel crosstalk penalty						0.2	dB	5
Rx signal input power (unamplified)	OSNR > 35dB/12.5GHz	100G DQPSK SC		-30		1	dBm	
		100G DQPSK RS		-24		1		
Rx signal input power monitor range			$P_{Rx,mon(s)}$	-21		3	dBm	
Rx signal input power monitor accuracy			$\delta P_{Rx,mon(s)}$	-2.5		2.5	dB	
Rx total input power monitor range			$P_{Rx,mon(t)}$	-21		6	dBm	
Rx total input power monitor accuracy			$\delta P_{Rx,mon(t)}$	-2.0		2.0	dB	
Rx reflectance						-20	dB	

Notes:

1. Rx signal input power range over which performance can be guaranteed with <1dB OSNR penalty relative to Rx OSNR tolerance limit.
2. Rx OSNR tolerance for Carrier Frequency Offset |CFO| < 1GHz. Up to 1dB penalty for worst case |CFO| = 3.6GHz.
3. Power dissipation will increase by approximately 0.2W if extended CD compensation is enabled.
4. Receiver is able to tolerate the specified ratio of total power of crosstalk channels and ASE to signal power with the specified OSNR penalty. Does not include contribution from adjacent channel crosstalk. No single channel power exceeding signal channel power by more than 1dB shall be included. Measured at Rx signal input power -6dBm.
5. Measured at the Rx OSNR limit, 50GHz channel spacing, both adjacent channels <1dB higher power than signal channel.

VII. Module Management Timing Characteristics

A. Common Management Interface Specification (CMIS) – DOLC335yS3PL1

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Note
Soft control and status functions							
MgmtInitDuration	Time from power on[1], hot plug or rising edge of reset until the high to low SDA transition of the Start condition for the first acknowledged TWI transaction.				2000	ms	1
ResetL Assert Time	Minimum pulse time on the ResetL signal to initiate a module reset.		10			µs	
IntL/RxLOS Mode Change Time	Time to change between IntL and RxLOSL modes of the dual- mode signal IntL/RxLOSL.				100	ms	
LPMode/TxDis Mode Change Time	Time to change between LPMode and TxDis modes of the LPMode/TxDis signal.				100	ms	
IntL Assert Time	Time from occurrence of condition triggering IntL until Vout:IntL=Vol				200	ms	
IntL Deassert Time	Time from clear on read[2] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.				500	µs	2
RxLOS Assert Time	Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted[3].				1	ms	3
RxLOS Deassert Time	Time from optical signal above the LOS deassert threshold to when the module releases the RxLOS signal to high.				15	ms	
Tx Disable Assert Time	Time from Tx Disable bit set (value = 1b)[4] until optical output falls below 10% of nominal				1	ms	4
Tx Disable Deassert Time	Time from Tx Disable bit cleared (value = 0b)[4] until optical output rises above 90% of nominal				10	s	4
Tx Fault Assert Time	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.				200	ms	
Flag Assert Time	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.				200	ms	
Mask Assert Time	Time from mask bit set (value=1b)[5] until associated IntL assertion is inhibited.				100	ms	5
Mask Deassert Time	Time from mask bit cleared (value=0b)[5] until associated IntL operation resumes.				100	ms	5
Data Path Tx Turn On Max Duration[6]	Maximum duration of Tx Turn On state.		see CMIS memory P01h: B168				6
Data Path Tx Turn Off Max Duration[6]	Maximum duration of Tx Turn Off state.		see CMIS memory P01h: B168				6
Data Path Deinit Max Duration[6]	Maximum duration of DataPathDeInit state.		see CMIS memory P01h: B144				6
Data Path Init Max Duration[6]	Maximum duration of DataPathInit state.		see CMIS memory P01h: B144				6
Module Pwr Up Max Duration[7]	Maximum duration of Module Pwr Up state.		see CMIS memory P01h: B167				7
Module Pwr Dn Max Duration[7]	Maximum duration of Module Pwr Dn state.		see CMIS memory P01h: B167				7

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Note
I/O timing for squelch & disable							
Rx Squelch Assert Time	Time from loss of Rx input signal until the squelched output condition is reached.				15	ms	
Rx Squelch Deassert Time	Time from resumption of Rx input signals until normal Rx output condition is reached.				15	ms	
Tx Squelch Assert Time	Time from loss of Tx input signal until the squelched output condition is reached.				400	ms	
Tx Squelch Deassert Time	Time from resumption of Tx input signal until the normal Tx output condition is reached.				10	s	
Rx Output Disable Assert Time	Time from Rx Output Disable bit set (value = 1b)[4] until Rx output falls below 10% of nominal				100	ms	4
Rx Output Disable Deassert Time	Time from Rx Output Disable bit cleared (value = 0b)[4] until Rx output rises above 90% of nominal				100	ms	4
Squelch Disable Assert Time	This applies to Rx and Tx Squelch and is the time from bit set (value = 1b)[4] until squelch functionality is disabled.				100	ms	4
Squelch Disable Deassert Time	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[4] until squelch functionality is enabled.				100	ms	4

Notes:

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified
2. Measured from low to high SDA edge of the Stop condition of the read transaction
3. RxLOS condition is defined as (a) Rx input power below threshold or (b) DSP loss of signal
4. Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction
5. Measured from low to high SDA edge of the Stop condition of the write transaction
6. Measured from the low to high SDA edge of the Stop condition of the Write transaction until the IntL for the state change Vout:IntL=Vol, unless the module advertises a less than 1 ms duration in which case there is no defined measurement.
7. Measured from the low to high SDA edge of the Stop condition of the Write transaction until the IntL for the state change Vout:IntL=Vol.

B. SFF-8636 Management Interface – DOLC335yR3PL1

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Note
Soft control and status functions							
Initialization time	Time from power on or hot plug until the module is fully functional (assuming LPMode pulled low by the host).				120	s	2, 3
Reset Init Assert Time	Minimum pulse time on the ResetL signal to initiate a module reset.		10			µs	
Serial Bus Hardware Ready Time	Time from power on until the module responds to data transmission over the two-wire serial bus.				2	s	2
Monitor Data Ready Time	Time from power on to Data_Not_Ready, Byte 2 bit 0, cleared to 0 and IntL output pulled low.				2	s	2
Reset Assert Time	Time from a rising edge on the ResetL input until the module is fully functional				120	s	3
LPMode/TxDis mode change time	Time to change between LPMode and TxDis modes of the dual-mode signal LPMode/TxDis.				100	ms	
LPMode Assert Time	Time from when the host releases LPMode to high until module power consumption reaches Power Class 1.				100	ms	
LPMode Deassert Time	Time from when the host pulls LPMode low until the module is fully functional.				120	s	3
IntL/RxLOSL mode change time	Time to change between IntL and RxLOSL modes of the dual-mode signal IntL/RxLOSL.				100	ms	
IntL Assert Time	Time from occurrence of condition triggering an interrupt until IntL is low.				200	ms	
IntL Deassert Time	Time from clear on read operation of associated flag until module releases IntL to high. This includes the time to clear Rx LOS, Tx Fault and other flag bits				500	µs	4
RxLOSL Assert Time	Time from optical loss of signal to RxLOSL signal pulled low by the module.				1	ms	
RxLOSL Deassert Time	Time from optical signal above the LOS deassert threshold to when the module releases the RxLOSL signal to high.				15	ms	
Tx Fault Assert Time	Time from Tx Fault state to Tx Fault bit set to 1 and IntL pulled low by the module.				200	ms	
Flag Assert Time	Time from condition triggering flag to associated flag bit set to 1 and IntL pulled low by the module.				200	ms	
Mask Assert Time	Time from mask bit set to 1 until the module is prevented from pulling IntL low when the associated flag is set high.				100	ms	1
Mask Deassert Time	Time from mask bit cleared to 0 until module is enabled to pull IntL low when the associated flag is set high.				100	ms	1
I/O timing for squelch & disable							
Rx Squelch Assert Time	Time from loss of Rx input signal until the squelched output condition is reached.				15	ms	
Rx Squelch Deassert Time	Time from resumption of Rx input signals until normal Rx output condition is reached.				15	ms	
Tx Squelch Assert Time	Time from loss of Tx input signal until the squelched output condition is reached.				400	ms	
Tx Squelch Deassert Time	Time from resumption of Tx input signals until normal Tx output condition is reached.				10	s	
Tx Disable Assert Time	Time from Tx Disable bit set to 1 until optical output falls below 10% of nominal.				1	ms	1

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Note
Tx Disable Deassert Time	Time from Tx Disable bit cleared to 0 until optical output rises above 90% of nominal.				10	s	1
Rx Output Disable Assert Time	Time from Rx Output Disable bit set to 1 until Rx output falls below 10% of nominal.				100	ms	1
Rx Output Disable Deassert Time	Time from Rx Output Disable bit cleared to 0 until Rx output rises above 90% of nominal.				100	ms	1
Squelch Disable Assert Time	This applies to Rx and Tx Squelch and is the time from bit cleared to 0 until squelch functionality is disabled.				100	ms	1
Squelch Disable Deassert Time	This applies to Rx and Tx Squelch and is the time from bit set to 1 until squelch functionality is enabled.				100	ms	1

Notes:
1. Measured from rising edge of SDA during STOP sequence of write transaction.
2. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level.
3. Fully functional is defined as the module being ready to transmit and receive valid signals and all management interface data, including monitors, being valid. It is indicated after Reset or hot plug by the module releasing IntL to high after the host has read a 0 from the Data_Not_Ready flag bit.
4. Measured from rising edge of SDA during STOP sequence of read transaction.

C. Optical

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Note
Tx turn on time	Warm start				10	s	1
	Cold start				120	s	
Rx acquisition time	Warm start				30	ms	
	Cold start				120	s	
Tx/Rx channel tuning time				10	30	s	

Notes:
1. Assumes the Tx/Rx laser is already tuned to the correct frequency.

VIII. Digital Management and Diagnostics Functions

The DOLC335yS3PL1 QSFP28 module supports the digital management and diagnostics interface specified in the Common Management Interface Specification (CMIS) [16] with extensions specified in the OIF Coherent CMIS implementation agreement [17].

The DOLC335yR3PL1 QSFP28 module supports the diagnostics and management interface specified in the Specification for Management Interface for 4-lane Modules and Cables SFF-8636 [18], with limited control and monitoring of the coherent line interface.

IX. Memory Contents

Per the Common Management Interface Specification (CMIS) [16] and the OIF Coherent CMIS implementation agreement [17] forDOLC335yS3PL1. Per the Specification for Management Interface for 4-lane Modules and Cables SFF-8636 [18] for DOLC335yR3PL1.

X. Mechanical Specifications

The DOLC335yx3PL1 (y = 2/3, x = R/S) QSFP28 mechanical specifications are compliant to the applicable standards [3-7], with exceptions for the mechanical dimensions of the front of the transceiver that extends outside the cage, which are aligned with the specifications for the Type 2 QSFP-DD form factor [8]. The pull tab color is White.

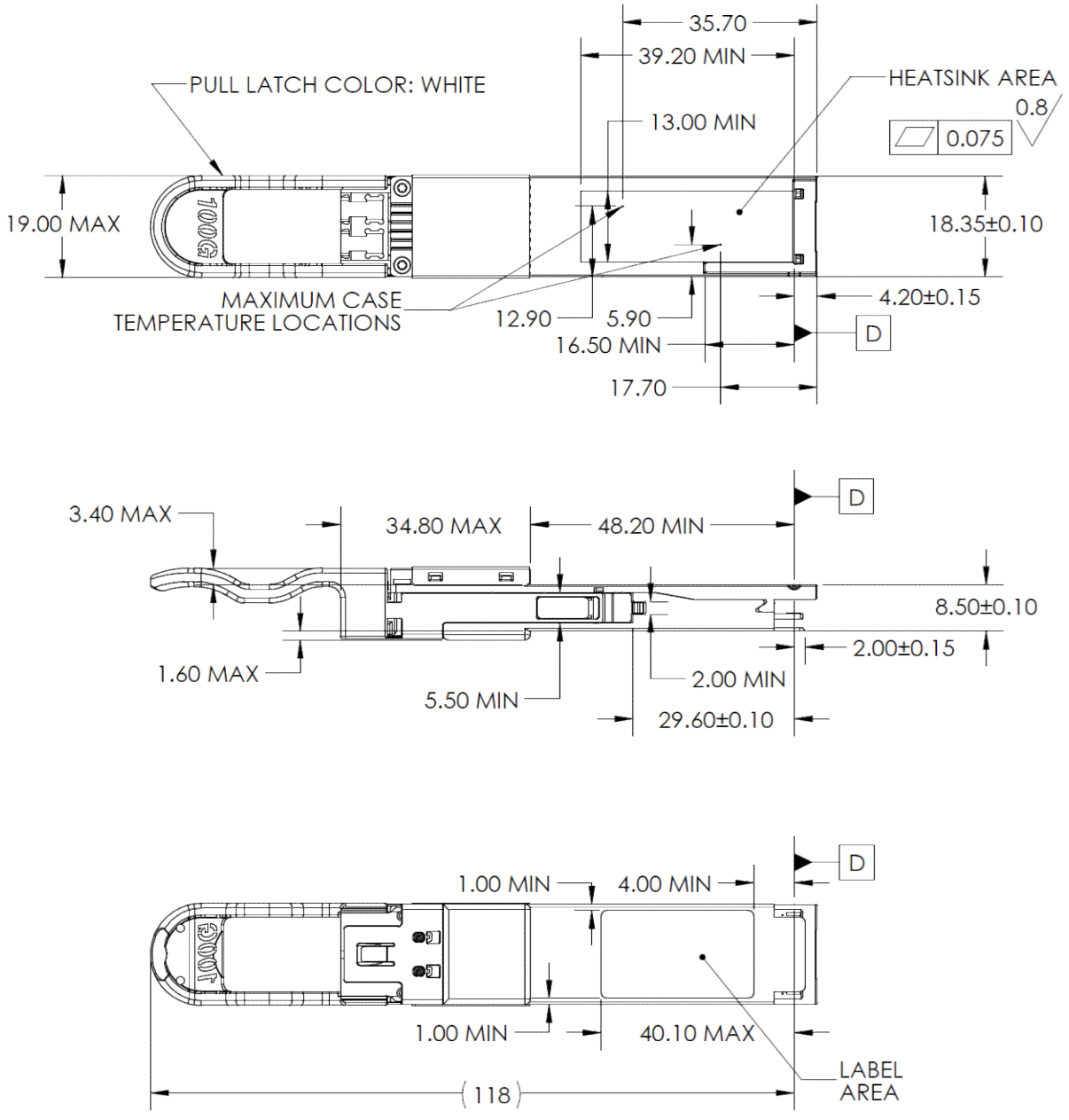


Figure 3 DOLC335yx3PL1 (y = 2/3, x = R/S) mechanical outline

XI. Regulatory Compliance

DOLC335yx3PL1 (y = 2/3, x = R/S) QSFP28-DCO transceivers are Class 1 Laser Products. They are certified per the following standards:

Feature	Agency	Standard
Laser eye safety	FDA/CDRH	CDRH 21 CFR 1040.10 and Laser Notice 56
	UL/CSA/TÜV	IEC/EN 60825-1:2014 IEC/EN 60825-2: 2004+A1+A2
Electrical safety	UL/CSA/TÜV	IEC/UL/EN 62368-1:2014

Copies of the referenced certificates will be available at Coherent Corp. upon request.

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

XII. References

1. SNIA “Specification for QSFP+ 28 Gb/s 4× Pluggable Transceiver Solution (QSFP28)”, SFF-8665 Rev. 1.9 (June 29, 2015).
2. SNIA “Specification for QSFP+ 4× Hardware and Electrical Specification”, SFF-8679 Rev. 1.8 (October 4, 2018).
3. SNIA “Specification for QSFP+ 4× Module” SFF-8661 Rev. 2.5 (June 22, 2018).
4. SNIA “Specification for QSFP+ 4× 28 Gb/s Connector (Style A)” SFF-8662 Rev. 2.9 (June 8, 2018).
5. SNIA “Specification for QSFP+ 28 Gb/s Cage (Style A)” SFF-8663 Rev. 1.7 (October 19, 2017).
6. SNIA “Specification for QSFP+ 4× 28 Gb/s Connector (Style B)” SFF-8672 Rev. 1.2 (June 8, 2018).
7. SNIA “Specification for QSFP+ Cage” SFF-8683 Rev. 1.3 (October 19, 2017).
8. QSFP-DD MSA “QSFP-DD/QSFP-DD800/QSFP112 Hardware Specification for QSFP Double Density 8× And QSFP 4× Pluggable Transceivers” Rev. 6.3 (July 26, 2022).
9. IEEE Computer Society “IEEE Standard for Ethernet”, IEEE Std 802.3-2022.
10. ITU-T “Interfaces for the Optical Transport Network” G.709/Y.1331 Ed. 6.3 (February 2022).
11. ITU-T “OTU4 Long-Reach Interface” G.709.2/Y.1331.2 Ed. 1.1 (September 2020).
12. ITU-T “Amplified Multichannel Dense Wavelength Division Multiplexing Applications with Single Channel Optical Interfaces” G.698.2 Ed. 3.0 (November 2018).
13. ITU-T “Characteristics of Optical Transport Network Hierarchy Equipment Functional Blocks” G.798 Ed. 6.6 (May 2022).
14. CableLabs “P2P Coherent Optics Physical Layer 1.0 Specification” P2PCO-SP-PHYv1.0-I03-200501 (May 2020).
15. OIF “Common Electrical I/O (CEI) - Electrical and Jitter Interoperability Agreements for 6G+ bps, 11G+ bps,25G+ bps, and 56G+ bps I/O”, OIF-CEI-4.0 (December 29, 2017).
16. OIF “Implementation Agreement – Common Management Interface Specification (CMIS)” OIF-CMIS-05.2 (April 2022).
17. OIF “Implementation Agreement for Coherent CMIS”, OIF-C-CMIS-01.3 (October 2023).
18. SNIA “Specification for Management Interface for 4-lane Modules and Cables”, SFF-8636 Rev 2.11 (January 3, 2023).
19. SNIA “Specification for SFF Module Management Reference Code Tables”, SFF-8024 Rev 4.10 (November 24, 2022).
20. Directive 2011/65/EU of the European Parliament and of the Council, “on the restriction of the use of certain hazardous substances in electrical and electronic equipment” as well as Commission Delegated Directive (EU) 2015/863 amending Annex II to Directive 2011/65/EU. Certain products may use one or more exemptions as allowed by the Directive.
21. Application Note AN-2038: “COHERENT Implementation of RoHS Compliant Transceivers”.